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Characterization of the demonstrator of the fast silicon monolithic ASIC for the TT-PET project

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Abstract: The TT-PET collaboration is developing a small animal TOF-PET scanner based on monolithic silicon pixel sensors in SiGe BiCMOS technology. The demonstrator chip, a small-scale version of the final detector ASIC, consists of a 3×10 pixel matrix integrated with the front-end, a 50 ps binning TDC and read out logic. The chip, thinned down to 100 µm and backside metallized, was operated at a voltage of 180 V. The tests on a beam line of minimum ionizing particles show a detection efficiency greater than 99.9% and a time resolution down to 110 ps.

Keywords: Pixelated detectors and associated VLSI electronics; Solid state detectors; Timing detectors; Gamma camera, SPECT, PET PET/CT, coronary CT angiography (CTA)

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1 The TT-PET ASIC

1.1 Challenges and previous results

The development of a monolithic silicon pixel detector with 30 ps RMS (70 ps FWHM) time resolution for 511 keV photons is the main challenge of the Thin-TOF PET (TT-PET) [1] scanner, a small-animal PET system that makes use of a stack of silicon sensors to detect electrons from converted photons. The strategy adopted for this chip, already described in [2], is to integrate the sensor and the front-end electronics in a SiGe BiCMOS process, to produce an ultra-fast, low-power silicon pixel detector. The ASIC will have a thickness of 100 µm, comprising the BiCMOS processing and a depletion depth of 80 µm on a high resistivity substrate. In order to saturate the drift velocity of the charge carriers and provide a very uniform weighting field, the sensor will be backside metallized and will operate with a high voltage of approximately 200 V. The large number of detection elements in a small animal scanner (1920 monolithic chips) sets a constraint on the power consumption to 200 µW/channel for $500 \times 500\,\mu m^2$ pixels.

The target of 30 ps RMS time resolution for electrons from the conversion of 511 keV photons corresponds to approximately 100 ps RMS for perpendicularly incident minimum ionising particles (MIPs), due to the smaller charge that MIPs generate into the sensor [2]. The first TT-PET ASIC prototype achieved a record time resolution for a monolithic pixel sensor of 220 ps RMS with MIPs, with a power consumption of 350 µW for $900 \times 450\,\mu m^2$ pixels [2]. That chip was operated on a 700 µm thick, high resistivity substrate, with a depletion depth of 150 µm. An improvement of a further factor two from this result is possible by reducing the sensor thickness at fixed detector capacitance and metallizing the backside of the chip, which will increase the uniformity of the weighting field for the induced current and saturate the drift velocity of the charge carriers [3, 4].

1.2 The demonstrator

The ASIC prototype described in this work, and hereby called demonstrator [5], is a monolithic chip developed for the TT-PET project in the SiGe BiCMOS process SG13S from IHP microelectronics [6]. The demonstrator, shown in figure 1, was designed to test the main elements of the final TT-PET chip.

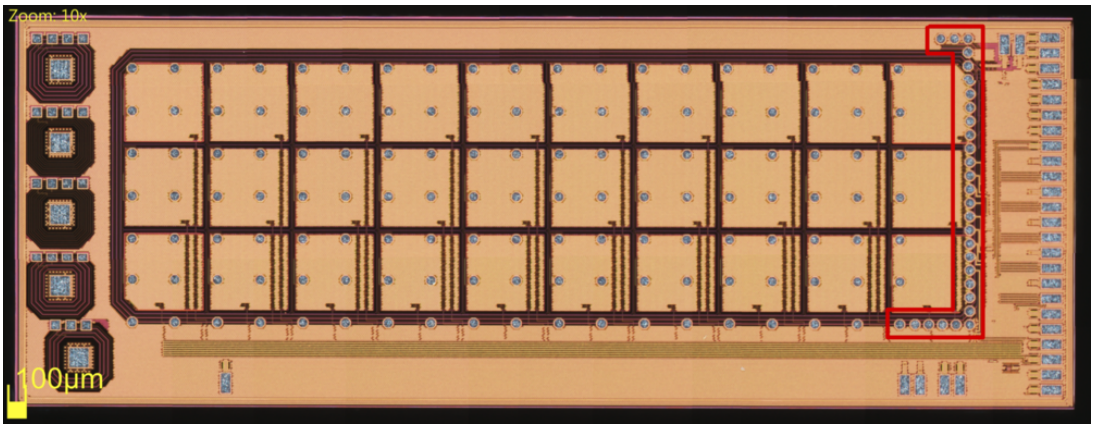

Figure 1. Microscope picture of the demonstrator of the fast monolithic silicon pixel detector of the TT-PET project. The pixel matrix consists of three rows of 10 pixels each. The guard ring is partially visible from the opening of the metallization around the pixel matrix. The signals from the pixels are routed to the front-end, distributed over the long side of the chip, outside the guard ring. The TDC, logic and I/O is in the right periphery of the chip. The rectangular wire-bonding pads are connected to smaller octagonal bump-bonding pads, sitting close to the edge of the rightmost pixel column (inside the area identified by the red lines). The five structures on the left are independent guard-ring test structures.

The ASIC comprises a matrix of 30 square n-on-p pixels of $470 \times 470\,\mu m^2$ area, with $30\,\mu m$ inter-pixel spacing. The positive high voltage is applied to the pixels, with a breakdown voltage of approximately 210 V. The depletion region extends for a depth of $82\,\mu m$ in the $1\,k\Omega cm$ resistivity substrate, limited by the backside thinning and metallization. This high voltage ensures the generation of an electric field in the sensor bulk above $2\,V/\mu m$. The large ratio between the pixel side and the sensor thickness is necessary to maximize the sensor uniformity of response in terms of timing [3, 7]. The signal generated in each pixel is routed to the front-end, placed outside the guard ring in the periphery of the chip.

The front-end comprises a pre-amplifier based on a SiGe HBT transistor and a CMOS-based open-loop tri-stage discriminator. The discrimination threshold can be adjusted independently for each channel with an 8-bit DAC. The output of the discriminator is sent to a fast-OR chain, which preserves the time of arrival and the time over threshold (TOT) of the pixel. The address of the pixel is also registered. Each pixel can be masked, in which case its signal does not propagate to the fast-OR. In this prototype, if two pixels in a chip fire in a single event, only the first time of arrival is registered, while the address of the pixel with the lowest row and column index is assigned to the hit. This simple architecture was chosen for the demonstrator as a robust solution to limit the complexity of the read out logic. In the final chip multiple independent fast-OR lines will be used to handle events with cluster size larger than one.

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The time of arrival and the time over threshold of the fast-OR output signal are digitized using a CMOS-based hybrid TDC made of a free-running ring oscillator with a binning of 50 ps and a 700 ps counter, developed on purpose for this project [8]. Both the counter and the 14 states of the ring oscillator are read for the measurement of the time of arrival and the time over threshold of the signal.

A 10 MHz clock is distributed to the different chips to offer a common time reference for the TDCs and run the chip logic.

2 Experimental setup and methods

2.1 The experimental setup at the SPS beam test facility at CERN

In order to study the efficiency, timing performance, front-end noise and uniformity of response, the demonstrator chip was tested at the SPS beam test facility at CERN with MIPs. The experimental setup (figure 2) consisted of a tracking telescope [9] that provided the trigger and the particle track parameters to three demonstrator chips. The three chips were read out using a readout system developed at the DPNC,[1] with a custom firmware designed to operate the demonstrator with an external trigger.

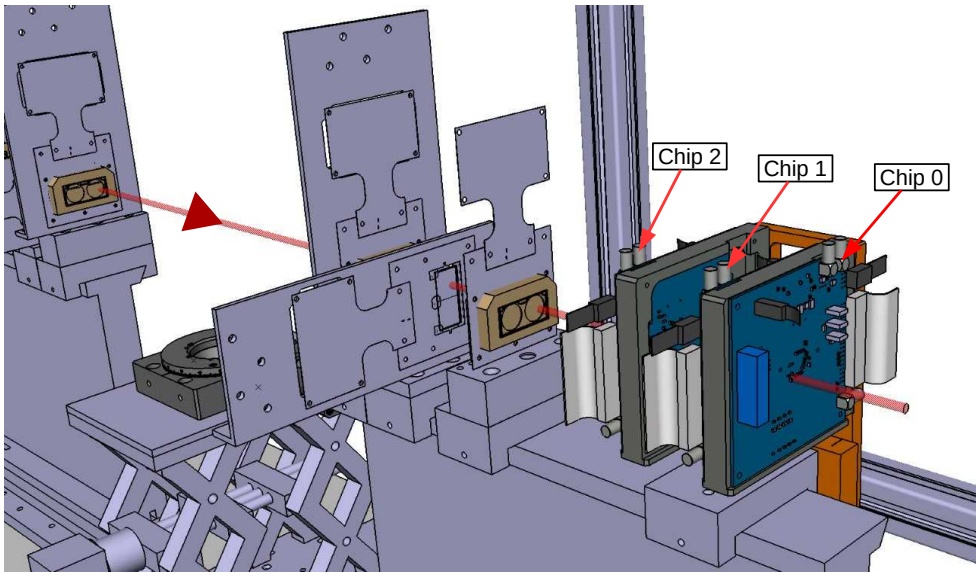

Figure 2. The experimental setup at the SPS beam test facility. The red line represents the particle beam. Four of the tracking telescope planes are visible on the left. The three boards with the demonstrator were downstream with respect to the telescope. The board containing chip 0 was rotated by 180 degrees along the vertical axis with respect to the other two boards.

The chips were operated at two working points: a low-power working point, with a preamplifier power consumption of 160 µW/channel, compliant with the TT-PET power requirements, and, for comparison, a working point with power consumption of 375 µW/channel, as was used for the previous monolithic prototype [2]. At higher power consumption the amplifier is expected to

[1] https://www.unige.ch/dpnc/en/.

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perform better in terms of gain and noise, thanks to the increased transition frequency of the transistor that leads to a better matching of the pixel capacitance. For both working points a high voltage of 180 V was applied during data taking.

The nominal threshold was set to 15 mV above the measured amplifier baseline, corresponding to approximately 5 standard deviations from the electronic noise for each pixel, with a calibration procedure that minimized the noise hit rate; it was then raised for the efficiency measurement as a function of the threshold. After the calibration, the noise hit rate per chip was measured to be 4.3×10^{-3} Hz at the nominal threshold. The coincidence time window with the telescope trigger was set to 200 ns, corresponding to a random hit probability per chip in the trigger window lower than 10^{-9}. The coincidence time window was set to the above value to take into account the delay and time jitter of the telescope.

During the data taking, the four pixels closer to the I/O pads (corresponding to the three pixels of the rightmost column in figure 1 and the bottom pixel in the adjacent column) were masked on hardware, due to noise induced on them by the single-ended clock line. The coupling between these pixels and the digital lines was caused by the vicinity of the I/O bump-bonding pads (the octagonal pads inside the red lines to the right side of figure 1), which were not used but still connected to the corresponding signals. These pads will be removed in the final chip and the clock will be distributed using differential lines.

The relative position of the three chips, measured using the particles of the beam and limited to the active pixels, is shown in figure 3.

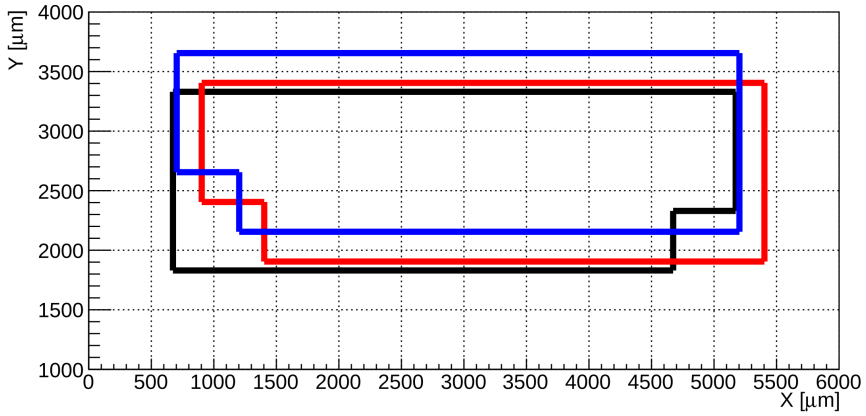

Figure 3. Relative position of the three demonstrator chips under test in the reference frame of the beam telescope. The active area of the chip 0 is delimited by the black line, of chip 1 by the red line and of chip 2 by the blue line.

2.2 Analysis of the data

To minimize the effects of the multiple scattering and of the tracking-telescope pointing resolution, for the efficiency calculation an area of 50 µm around the edge of the active area of the chip, comprising the region of the pixels closest to the first guard ring, was removed from the analysis. The same exclusion area was used for the calculation of the time resolution.

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A cut was applied during the analysis to remove the effect of a small issue, that has been identified thanks to this prototype: due to a minor design flaw of the TDC, the counter had an uncertainty of 1 bit for the events recorded in one of the fourteen states of the TDC ring oscillator. For this reason, the events in bin 9 of the TDC ring oscillator in figure 4 were removed from the analysis. This selection reduces the available statistics without introducing a bias on the data sample, since the time of arrival of the hit is asynchronous with respect to the phase of the TDC ring oscillator. This error will be corrected in the final chip design.

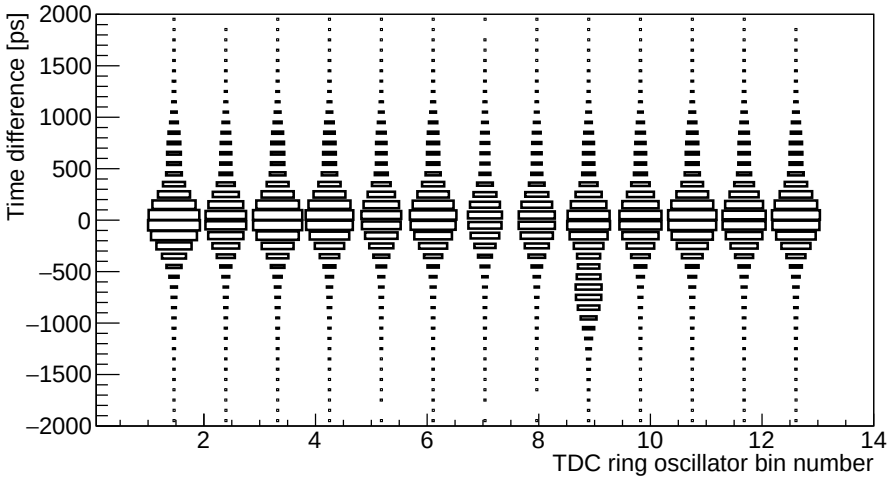

Figure 4. Time difference between chip 0 and chip 1 as a function of the status measured by the TDC ring oscillator. The counter starting-time uncertainty, visible for bin 9, causes a systematic error of one period of the ring oscillator, corresponding to 700 ps.

3 Results

3.1 Efficiency and front-end noise

The efficiency of the three chips under test was measured for the two amplifier power consumption working points. The results obtained at the nominal threshold are reported in table 1. When calculating the efficiency, to reduce further the effect of the multiple scattering and of the beam-telescope resolution near the chip border, a hit confirmation was requested on the other two chips under test. The efficient events are those for which a hit was acquired within the coincidence window by the chip under study.

Figure 5 shows the pixel efficiency for the chip in the center (chip 1), measured at the nominal threshold value for the low-power working point. The line in the figure indicates the borders of the area used to calculate the efficiency.

Figure 6 shows the efficiency of chip 1 measured at different thresholds at the low-power operating point. The data show the noise margin for sensor operation, with the efficiency plateau extending over a factor two above the nominal discriminator threshold. These data, obtained with minimum ionizing particles crossing perpendicularly the sensor, are compatible with an amplifier gain of (50 ± 5) mV/fC. This estimation was done for the depletion depth of 82 µm, for which the

Table 1. Efficiency at nominal threshold for the three demonstrator chips under test for different values of the amplifier power consumption. Only the statistical error is reported. The two values of the power consumption correspond to the working point of the front-end for the TT-PET scanner (160 µW/ch) and the working point used for testing the previous prototype [2] (375 µW/ch).

Power consumption [µW/ch]	Efficiency [%]		
	Chip 0	Chip 1	Chip 2
160	99.933 ± 0.007	99.986 ± 0.003	99.985 ± 0.003
375	99.924 ± 0.006	99.980 ± 0.003	99.973 ± 0.003

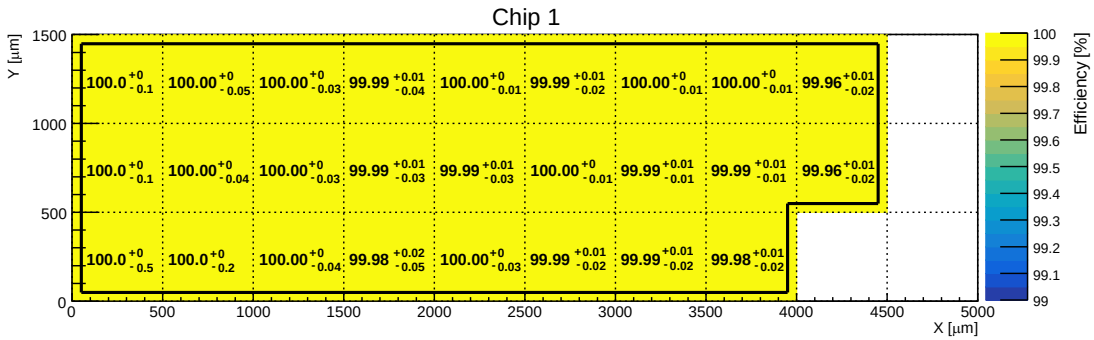

Figure 5. Pixel efficiency map of chip 1. The colored area is the chip active area. The dashed lines represent the separation between pixels. The continuous line represents the border of the area used for the efficiency calculation. The four pixels in white were masked in hardware as discussed in the text.

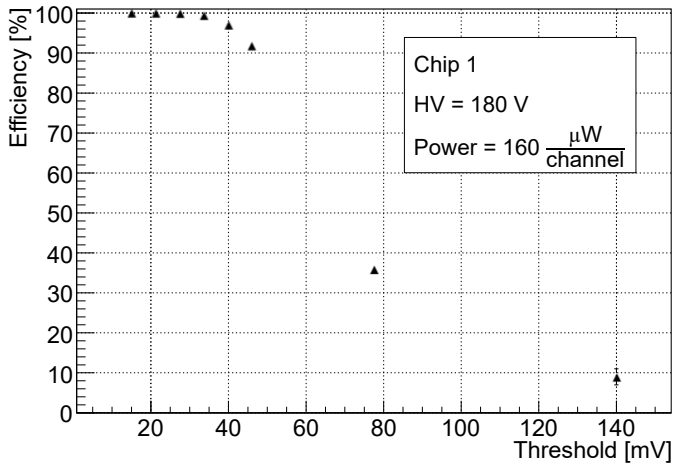

Figure 6. Efficiency as a function of the voltage threshold for chip 1. The voltage threshold value shown in the horizontal axis represents the difference between the global threshold setting and the typical voltage offset at the output of the preamplifier. The mismatch between different channels is corrected with the pixel DAC. For the nominal working point the threshold was set to 15 mV above the amplifier baseline.

most probable collected charge was simulated to be 0.91 fC and the minimum charge for particles hitting at the center of the pixel was approximately 0.55 fC.

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The equivalent noise charge (ENC) of the front-end was estimated from the gain and noise rate measured at the nominal threshold.[2] The nominal threshold, Vth_{min}, corresponds to at least 5 standard deviations of the amplifier voltage noise (compatible with such a small noise hit rate and in accordance to bench measurements described in [5]). The front-end ENC can be estimated as:

$$\text{ENC} = \frac{\frac{Vth_{\text{min}}}{N_{\sigma_{\text{noise}}}}}{\text{Gain}} \approx 350\ e^{-}$$

where $N_{\sigma_{\text{noise}}} = 5$ is the number of standard deviations of the voltage noise corresponding to the nominal threshold. Therefore the nominal threshold of 15 mV corresponds approximately to 1750 e^{-}.

3.2 Time resolution

Figure 7 left shows the distribution of the signal TOT for the hits recorded by one of the pixels of chip 1 at the low-power working point. Different TOT peaks are visible in the figure and they can be attributed to different reasons. We attribute the first peak, visible between 3 ns and 7 ns, to a non linear response of the discriminator for the smallest signals. The main peak, at 12 ns, corresponds to the most probable charge deposited into the sensor by a MIP. It is followed by secondary peaks at 14 ns and 17 ns. A possible explanation for these peaks is a small residual noise induced by the single-ended digital trigger signal, affecting the grounding of the pixel matrix. In this scenario, the time difference between the peaks would be caused by the delay of the fast-OR line. The first peak between 3 and 7 ns, visible with MIPs, should not be present when operating the sensor with more ionizing radiation, as in the case of the TT-PET scanner. The digital cross-talk, on the contrary, can be reduced only improving the design at system level. The introduction of slower trigger signals in a differential configuration in the final chip will eliminate this problem.

For the calibration and measurement of the time resolution, hits with a TOT between 2 ns and 40 ns were selected. The time calibration consisted of two steps: the time-walk correction and the time-skew correction. As an example, figure 7 right shows the time difference between chip 1 and chip 0 as a function of the TOT of chip 1, for one of the pixels of chip 1. These distributions were used for the time-walk correction. The green segments represent the mean value of the time difference for TOT slices of 0.25 ns. These mean values were fitted with two polynomial curves. The use of different curves for different TOT intervals is motivated by the non linear response of the discriminator for the smallest signals. The range of the time-walk correction spans approximately 1 ns, making this calibration fundamental to obtain a 100 ps time resolution.

The time skew between different pixels of the same chip is mostly generated by the different path of the signals in the fast-OR line. To correct for this effect, the average time of arrival, corrected for time-walk, is set to the same value for each pixel. The initial time-skew between two pixels was measured to be as large as 2 ns and is affected by the mismatch of the electronic components.

The time resolution can be obtained by measuring the jitter of the time of flight between two calibrated chips. Figure 8 shows the difference of the time of arrival between chip 0 and chip 1 for the low-power (left) and high-power (right) working point. The mean value, not significant for this study, was set to zero. The core of the distributions was fitted with a gaussian function in the

[2]This estimation of the ENC using the discrimination threshold is affected by the discriminator response, that shows a non-linearity for the smallest signals, effectively filtering part of the amplifier noise and decreasing the nominal threshold. The ENC of the amplifier, that contributes to the detector time resolution, is expected to be higher, as calculated in [5].

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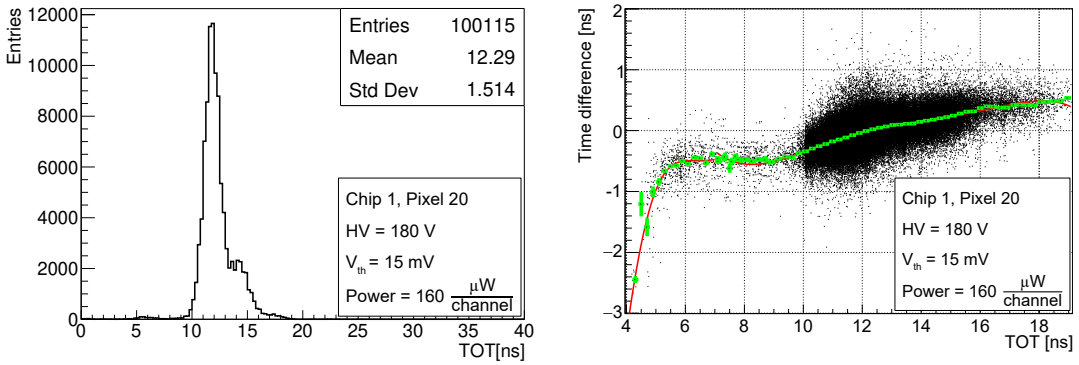

Figure 7. (Left) Signal time over threshold distribution for one of the pixels of chip 1. (Right) Example of time-walk correction function for one of the pixels of chip 1. The red lines are the result of a polynomial fit of the mean values of the time difference for TOT bins of 0.25 ns, represented by the green dots.

±2 standard deviations interval. The non-gaussian behavior of the tails was then measured as the fraction of events exceeding the gaussian functions in the entire range. The non-gaussian part of the tails was found to be a few percent.

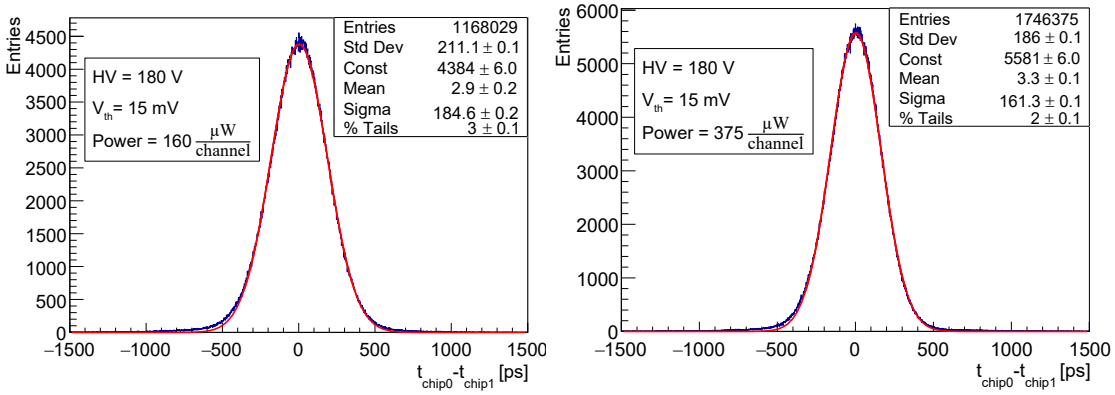

Figure 8. Time difference between chip 0 and chip 1 for an amplifier power consumption of 160 µW/channel (left) and 375 µW/channel (right).

Table 2 shows the resolution of the time of flight for the combinations of the three chips at the two working points as well as the corresponding single-detector time resolution. The three detectors show similar timing performance.

To give an idea of the uniformity of response within a chip, figure 9 shows the map of the time resolution of the pixels of chip 1 for the high-power working point. The map was obtained selecting the tracks that pointed to each pixel and measuring the time resolution using chip 0 as reference. To obtain the contribution from chip 1, the jitter of the time of flight was divided by $\sqrt{2}$. A steady small worsening of the time resolution towards the left of the map is visible. An hypothesis to explain this effect is the larger impedance of the ground line for the front-end channels far from the chip ground connection that is done in the right side of the chip.

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Table 2. (Left) Resolution of the time of flight between the three combinations of the chips under test. The σ is the standard deviation of the gaussian fit to the ±2 standard deviations core of the time-of-flight distribution. (Right) Time resolution of the three chips under test, obtained from the measurement of the time-of-flight resolution.

	TOF resolution [ps]	
	low-power	high-power
$\sigma_{\mathrm{TOF},0-1}$	184.6 ± 0.2	161.3 ± 0.1
$\sigma_{\mathrm{TOF},0-2}$	180.0 ± 0.2	157.3 ± 0.1
$\sigma_{\mathrm{TOF},1-2}$	184.9 ± 0.2	161.2 ± 0.1

	Time resolution [ps]	
	low-power	high-power
$\sigma_{t,\ \mathrm{chip\ 0}}$	**127.3 ± 0.2**	**111.3 ± 0.1**
$\sigma_{t,\ \mathrm{chip\ 1}}$	**134.2 ± 0.2**	**116.7 ± 0.1**
$\sigma_{t,\ \mathrm{chip\ 2}}$	**127.2 ± 0.2**	**111.2 ± 0.1**

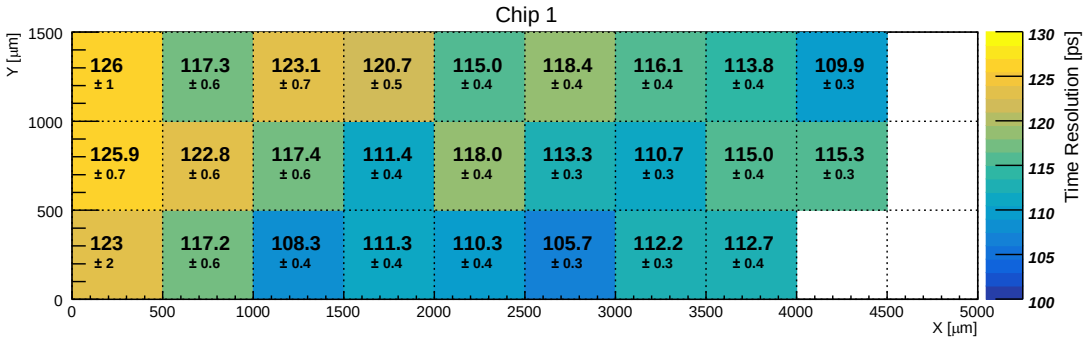

Figure 9. Time resolution of the pixels of chip 1. The dashed lines represent the separation between different pixels. The map shows the pixel matrix oriented as in figure 1. The error is statistical only.

4 Conclusions

The demonstrator of the fast, monolithic ASIC of the TT-PET project was produced and tested with minimum ionizing particles. The biasing structures, the pixel matrix, the fast-OR line and the TDC were qualified and the minor modifications required for the final chip design were identified. The measurements, done at a low-power (160 μW/channel) and a high-power (375 μW/channel) working point, show an efficiency above 99.9 % when the chip was operated at the nominal threshold of 15 mV, with a noise hit rate per chip of 0.004 Hz. The front-end noise, estimated from the efficiency measurement, is 350 e^- RMS. At the low-power working point, compatible with the power-budget of the TT-PET scanner, the time resolution was measured to be 130 ps RMS. A time resolution as low as 110 ps RMS was measured at the high-power working point, showing an improvement of a factor 2 with respect to the results of the first prototype of the TT-PET chip.

Acknowledgments

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