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# JICG CMOS transistors for reduction of total ionizing dose and single event effects in a 130 nm bulk SiGe BiCMOS technology

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ABSTRACT

We report on a novel radiation hardening by design (RHBD) approach for mitigation of total ionization dose (TID) induced drain leakage currents and single event transient (SET) in digital circuits fabricated in a 130 nm bulk SiGe BiCMOS technology. In order to avoid significant TID induced increase of drain leakage currents for NMOS transistors and channel pinch-off for PMOS transistors due to positive charges trapped at the lateral shallow trench insulator silicon interface we introduced junction isolation (JI) for the lateral MOS channel regions. The device construction measures applied also support to suppress the generation SETs. The tolerance of JI MOS transistors against TID induced drain leakage currents was verified up to a TID > 1.3 Mrad(Si). SET tests performed at four different inverter types varying in the arrangement the deep well in the layout. For CMOS inverters with isolated NMOS transistors a LET threshold > 130 MeV cm$^2$ mg$^{-1}$ was obtained.

## 1. Introduction

The SET robustness of MOS transistors in digital circuits can be improved by reduction of the amount of excess minority charge carriers collected by the reverse biased drain region and by reduction of the body contact and sheet resistance to avoid that the parasitic bipolar transistor, which operates in parallel to the MOS transistor, will be turned on. The turn on of the parasitic bipolar is controlled by the excess majority charge carriers which flows towards the body contact, rising the potential in the body region next to the source region. A review of the basic mechanisms for SETs in digital circuits can be found in [1].

Triple well bulk CMOS technologies enable to form p-wells, n-wells and deep n-wells. The additional implementation of a deep n-well enables the design of substrate isolated NMOS, and PMOS with reduced n-well (body) sheet resistance. Due to the improved substrate isolation of the NMOS the propagation of substrate noise on chip is significantly reduced. Deep n-wells strongly affect the amount of charge collection and the dynamics of charge distribution and charge sharing between sensitive circuit nodes after particle strike. While a deep n-well reduces the parasitic PNP base resistance and gain for PMOS, for isolated NMOS the NPN base resistance and gain will be somewhat increased because the p-well (body) sheet resistance of the NMOS is increased by compensation of the p-well doping by donors diffused from the deep n-well towards the surface. On the other hand the reverse biased deep n-well p-substrate junction also helps to collect a significant portion of excess charge carriers generated in the deeper MOS device region. Thus, a deep n-well causes a reduction of minority charge collected at the NMOS drain. The PMOS benefits from a deep n-well due to a reduced n-well sheet resistance which suppresses the turn on of the parasitic PNP. Overall the SET robustness of a digital circuit depends on many technology specific factors such as junction profiles, well depths and operating voltages. Depending on design and process an implemented deep n-well can potentially improve or even degrade the single event response of a digital circuit [2,3]. In [4] the authors report on intensively performed simulation studies on single event effects in digital CMOS circuits and review the status of SET simulation methodology in detail. 2-D simulations can provide only a qualitative basic insight in the creation of SETs. To obtain truly predictive quantitative results for submicron CMOS circuits 3-D simulation with valid mobility modes at high carrier concentrations and high concentrations gradients is necessary [5]. The results of a simulation study applied to a twin well 130 nm bulk CMOS process [6] show that PMOS charge sharing can be effectively mitigated using contacted guard-rings, whereas a combination of contacted guard-ring, nodal separation, and interdigitation helps to reduce the NMOS charge sharing effect. It was also demonstrated that charge sharing between adjacent devices can significantly increase Single Event Upset (SEU) vulnerability of digital circuits.

Ionizing radiation in high dose ranges > 1 Mrad can cause strong degradations of important MOS transistor parameters such as drain leakage current, threshold voltage, saturation current and switching speed. MOS transistors with narrow gate widths are especially affected

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by TID induced changes of MOS parameters. The positive fixed charge at the STI interface of MOS devices after an exposure to ionizing radiation laterally depletes the channel of PMOS devices while NMOS devices show increased source drain leakage due to an enhancement of negative inversion charge in the lateral channel region next to the positively charged STI interface. The countermeasure mostly applied to mitigate TID induced changes of MOS channel conductivity are enclosed layout transistors (ELTs) [7,8]. But ELTs have significant drawbacks. ELT is an unsymmetrical device, i.e. source and drain terminals cannot be simply mixed in the circuit. The minimum channel width of ELTs is limited by the minimum gate perimeter which can be drawn according to the layout rules of the underlying technology. Here, we introduce lateral junction isolation (JI) for the MOS channel to avoid TID induced leakage currents. This approach maintains the source drain symmetry of the MOS transistor and enables the design of devices with small gate widths.

Here we present the results of an experimental study in a triple well 130 nm bulk CMOS technology for mitigation of TID induced MOS parameter degradation and SET on device level. The TID tolerance of 1.2 V core and 3.3 V I/O MOS transistors with different levels of junction isolation was evaluated. Four different inverter constructions were tested for their SET tolerance. Our work aims to identify crucial device construction details for the design of additional rad hard digital library elements with significantly increased radiation tolerance for applications in harsh environments.

## 2. Experiment

A test chip utilizing 4 types of inverter chains with 2200 single stages was used for SET testing. For TID testing for each transistor type of core and I/O NMOS and PMOS transistors arrays of 49 single transistors connected in parallel were designed. The large total gate with of the TID test arrays is essential to prevent from ESD controlled device degradation during TID experiments in the usually harsh environment at the TID test site. All test devices were fabricated in the IHP 130 nm bulk SiGe BiCMOS technology SG13RH using the deep n-well option. All wells are implanted in a 3.7 μm thick p-type 20 Ω cm epitaxy layer. The CZ p Boron <100> substrate has 50 Ω cm substrate resistivity.

(a) TID Mitigation

TID induced source drain leakage at the STI walls was mitigated by lateral junction isolation (JI) of the MOS transistor channel.

JI MOS transistors have additional p-well regions of a width Δxj between the MOS channel beneath the gate and the STI walls. This enables to decouple the MOS channel from the TID induced parasitic n-channels at the STI walls. Taking into account the outdiffusion of the source drain regions a sufficiently great width Δxj prevents from a short circuit between the MOS channel and the parasitic n-channel at the STI walls. Thus, a TID induced increase of drain leakage current can be suppressed. The trapped positive fixed charge at the STI walls after irradiation influencing a parasitic n-channel is mainly a problem for NMOS transistors with narrow channel widths. PMOS transistors are not significantly affected. A finely structured silicid blocker layer protects against an electrical short at the surface where source drain regions are surrounded by body regions. Advanced litho processes enable a complete silicidation of the gate poly and to put the body contact in the same ACTIVE very close to the source region. Fig. 1 shows a layout of two inverter stages with isolated NMOS and PMOS with a lateral junction isolation of the MOS channels and a low resistance body connection in the same ACTIVE. Due to the lateral outdiffusion of the source/drain regions during the high temperature annealing steps following the source/drain and lightly doped drain (LDD) implantations the effective MOS channel width is increased by around 160 nm compared with the drawn value in the layout. Provided that a similar area is spent for contacts in the same ACTIVE, to obtain a low resistance body connection, for transistors widths w > 2 μm JI MOS transistors and ELTs show a similar space consumption. Fig. 2 shows a SEM image

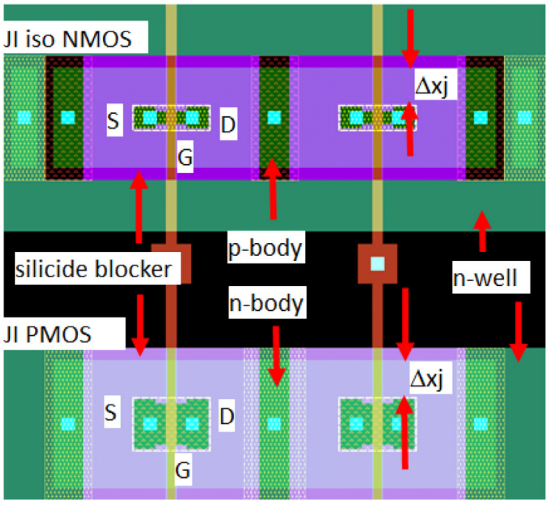


**Fig. 1.** Inverter layout with isolated NMOS and PMOS. Lateral junction isolation (JI) of MOS channels is adjusted by the distance of source/drain regions to STI edge Δxj.

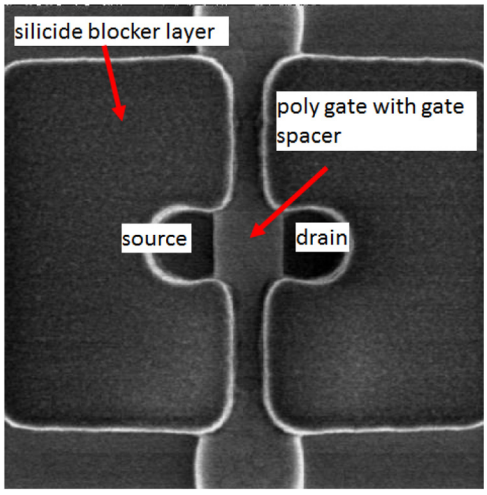


**Fig. 2.** SEM image of a JI iso NMOS before silicid blocker etch.

of a NMOS with a finely structured silicid blocker resist. Note, the gate is completely open enabling a complete silicidation as a prerequisite for a low gate resistance.

The body contact region is very close to source and drain and isolated by the silicide blocker layer. The resulting low body sheet resistance is essential to suppress the turn on of the parasitic bipolar transistor thereby reducing the SEE induced failure current at the drain.

**TID tests with $^{60}$Co-rays**

The gamma irradiation was carried out at the Helmholtz Institute (Helmholtz Zentrum Berlin, HZB) in Berlin, Germany.

The gamma quanta have energies of 1.173 and 1.332 MeV. In order to avoid that low-energy scattered radiation cause an inhomogeneous dose distribution, test specimens were surrounded by equilibrium material. The shielding material minimizes local dose enhancement from low-energy scattered radiation by producing charged-particle equilibrium. Container made of 1.5 mm Pb with an inner lining of 0.7 mm Al were used [9] which enclose the TID test boards. The samples were measured before and immediately after irradiation.

All samples were irradiated at room temperature for 160 h. The core and I/O NMOS transistors were biased with Vgs = Vdd at Vds = 0 V. For the PMOS all terminals were grounded. The total dose for each sample was adjusted by mounting the TID test boards in a defined radial

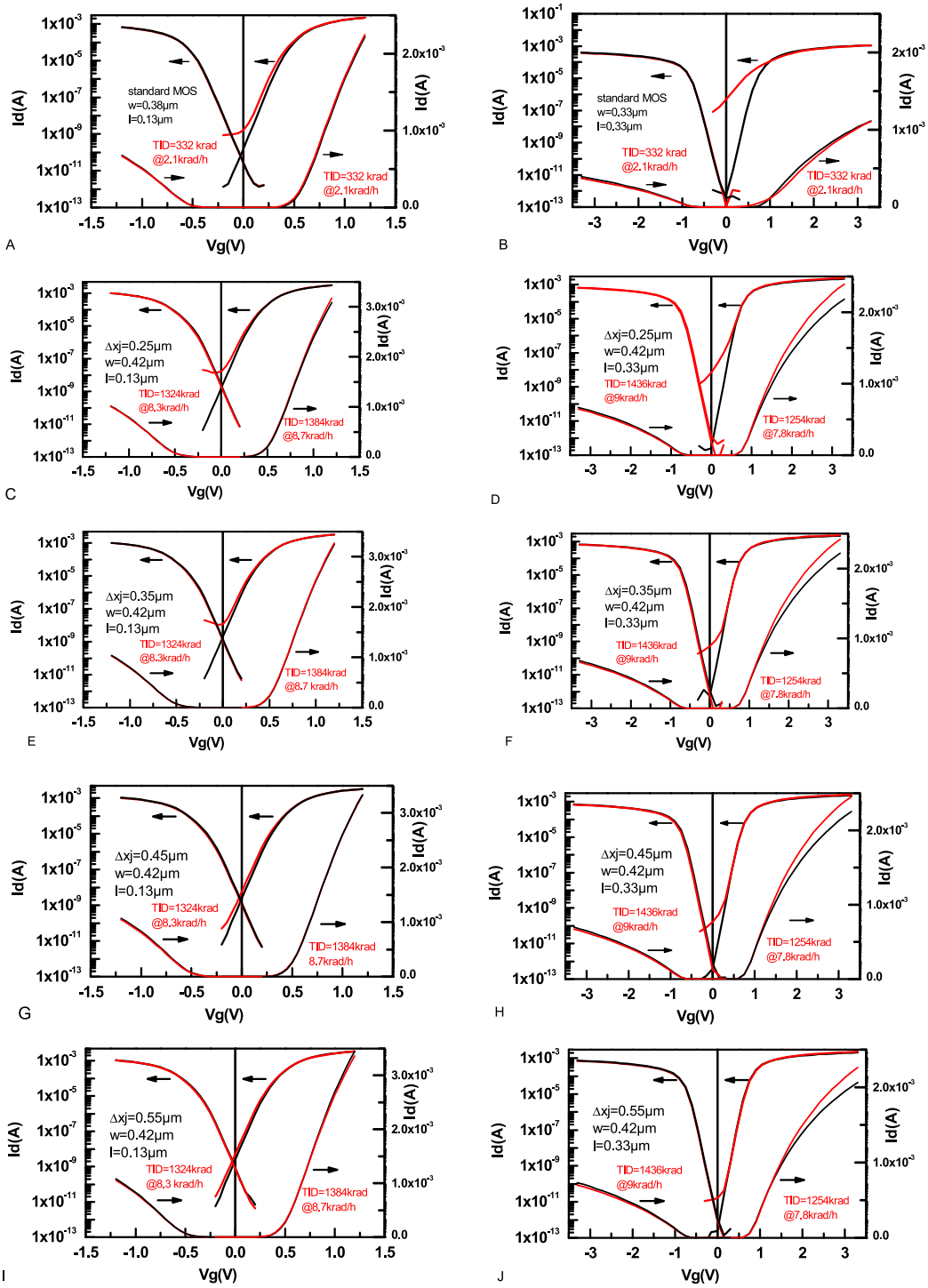


**Fig. 3.** TID induced degradation of transfer characteristics @ Vd = |0.1| V for standard (A , B) and junction isolated (D–J) core (left) and I/O (right) MOS transistors. The plotted Id(Vg) characteristics were measured at arrays with 49 single transistors. The single device channel width w as shown in each plot is the drawn value in the layout. Note, that due to the outdiffusion of the source/drain regions the effective gate width of the junction isolated MOS transistors is around 160 nm greater than their drawn layout values. Therefore the effective isolation width Δxj at each side of the MOS channel is reduced by around 80 nm in comparison to the drawn values as inserted in the single plots. For all core and I/O PMOS transistors TID induced MOS parameter degradation is negligible while core and I/O NMOS transistors show a sufficiently low drain current leakage for a junction isolation width Δxj > 0.45 µm (see Fig. 4).

distance from the 60Co source. Thus the dose rate varies with the radial distance of the samples from the 60Co source, i.e. the sample placed very close to the source receives the greatest dose at highest dose rate and vice versa the sample with the greatest distance from the source receives the lowest dose at lowest dose rate.

On each test board commercially available pellet dosimeters (4.8 mm diameter, 2.8 mm height) containing the Amino acid L-alpha alanine were mounted. During exposure to ionizing radiation stable free radicals are created in the dosimeter pellets. After irradiation the concentration of these free radicals was measured as microwave response of the pellet placed in the magnetic field of a paramagnetic resonance spectrometer. The spectrometer response is a measure for the radiation dose absorbed by the dosimeter pellet. The precision of this dosimetry is <1%. The total dosimetry error can be estimated to

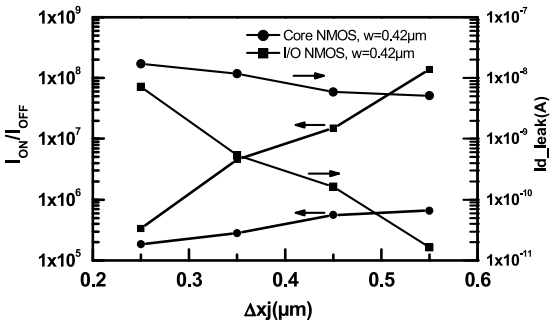


**Fig. 4.** Improvement of NMOS $I_{ON}/I_{OFF}$ drain current ratio and drain leakage current in dependence from the channel separation width Δxj. Δxj is the drawn value in the layout.

be lower than 10%. The functional dose range covered by using of dosimeter pellets is from 10 krad(Si) to 7 Mrad(Si).

The effectiveness of lateral junction isolation (JI) for the core and I/O transistors was evaluated by comparison of 4 values for the MOS channel separation width Δxj = 0.25 µm/0.35 µm/0.45 µm/0.55 µm. Each TID test transistor array was bonded in an open DIL 24 pin package and mounted on TID test boards. Fig. 3 shows the degradation of transfer characteristics of 49 single transistors connected in parallel in an array measured @ Vd = |0.1| V for standard (A and B) and junction isolated (C–J) core and I/O MOS transistors after exposure to ionizing radiation.

In comparison with standard core MOS transistors (A) core JI MOS devices (C, E, G, I) generally show increased OFF drain currents due to the increased areas of reverse biased drain-body pn-junctions. A significant lateral outdiffusion of the source drain regions gives electrical channel widths which are around 160 nm greater than drawn values in layout. This means that JI MOS transistors with electrical channel widths < 250 nm cannot be simply fabricated due to source drain lithography mask limitations. Expecting that the standard MOS devices will show the greatest TID induced parameter degradations already at moderate TID values, these were placed in a greater distance from the 60Co source than the junction isolated devices. Standard core and standard I/O PMOS transistors do not show any significant TID induced MOS parameter degradations. While standard core NMOS show @TID = 332 krad(Si) still a moderate increase of drain leakage lower than one order of magnitude standard I/O NMOS show a strong increase of drain leakage by more than five orders of magnitude. To prevent the core NMOS from significant TID induced MOS parameter degradations up to a TID = 1324 krad(Si) a separation of the MOS channel from the STI edge Δxj > 0.45 µm is sufficient. For the most sensitive I/O NMOS up to a TID= 1254 krad(Si) a channel separation Δxj > 0.55 µm reduces the increase of drain leakage to one order of magnitude. Fig. 4 shows the $I_{ON}/I_{OFF}$ drain current ratio and drain leakage current vs. the channel separation width Δxj.

Our criterion for digital applications in harsh environments is an acceptable low drain leakage level after irradiation, which still enables an $I_{ON}/I_{OFF}$ drain current ratio > $5 \times 10^5$.

(b) SET Mitigation

With ongoing technology scaling the device density increases while less charge is required for generation of SETs. In order to save chip area usually MOS transistors are arranged tightly together in parallel or serial blocks which represent a certain logical functionality such as NAND or NOR. In such dense arrangements charge sharing between the single transistors in logical blocks becomes a severe problem because a single particle strike can now simultaneously disturb the blocking capability of several transistors resulting in multiple malfunction of a logical gate.

For the SET tests we used a simple inverter chain arrangement composed of a chain of 2200 single JICG inverters. AS sown in Fig. 5

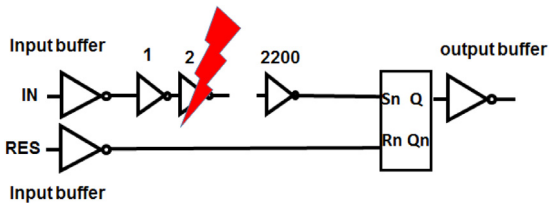


**Fig. 5.** Inverter chain test circuit for SET testing.

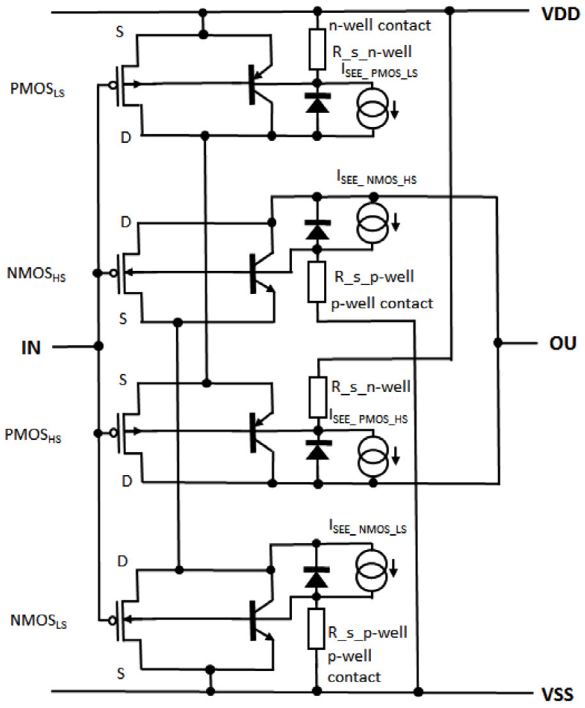


**Fig. 6.** Circuit scheme of stacked CMOS inverter illustrating the impact of SEE induced charge collection in the sensitive regions of the single transistors. The circuit scheme illustrates the arrangement of the single NMOS and PMOS transistors in the layout. The SEE test inverter arrangement is composed of two NMOS and PMOS transistor stacks sharing a common gate (CG). Each MOS stack consists of a low side device (LS) and a high side (HS) device serially connected. The vertical distance between the single transistors is 3.7 µm (see layout in Fig. 1). For the NMOS/PMOS low side device the source is connected to $V_{SS}/V_{DD}$.

the last inverter output is connected to an RS-latch to catch propagated SETs.

The experimental setup used for initializing and SET counting is based on a modular PXI test system from National Instruments. Fig. 6 shows a detailed circuit scheme of a single inverter.

The gate width for the NMOS is $w_N$ = 0.3 µm and for the PMOS $w_P$ = 0.64 µm. All transistors in the inverter are junction isolated (JI) with Δxj = 0.45 µm (see Fig. 1). The isolating well regions completely surround the source drain regions. The large well contact bars right and left are located in the same ACTIVE which gives a very low sheet and contact resistance for the body connection (see Fig. 1). To suppress the turn on of the parasitic bipolar transistors operating in parallel to the source drain regions of each MOS transistor a low sheet and contact resistance of the body is essential. Thus the constructive measures of isolating well regions for suppressing TID induced leakage at the STI walls also help to decrease the vulnerability against SEEs. For the simulation of the behaviour of serially connected transistors as to be found in the serial NMOS block of NAND gates or in the serial PMOS block of NOR gates each transistor in the inverter is replaced by a stack of two transistors sharing a common gate (CG). Each NMOS and PMOS stack consists of a low side (LS) and a high side (HS) device. The vertical geometrical distance between the drain regions of a low side and a high side device

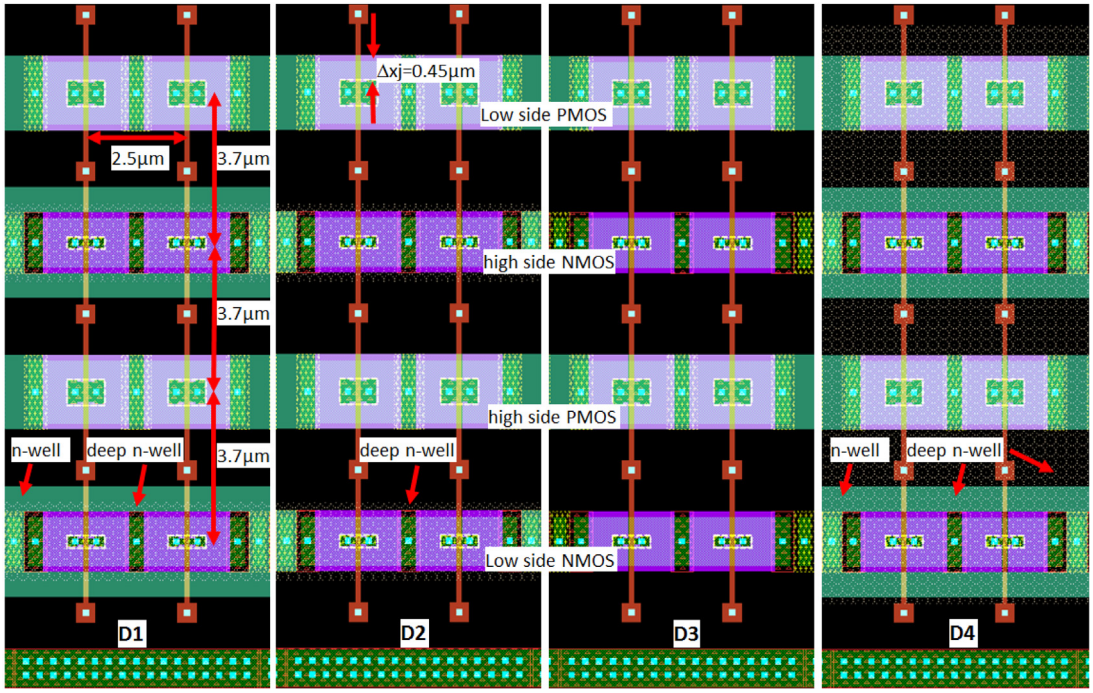


**Fig. 7.** Four different inverter layouts D1, D2, D3, D4 used for SET testing. The distance of source/drain regions to STI edge Δxj for a lateral junction isolation of the MOS channel is for all four designs 0.45 µm.

is 7.4 µm. The source of a high side device is connected with the drain of the corresponding low side device. The horizontal distance of two adjacent inverters is 2.5 µm (see Fig. 1).

It is worth to note that in bulk CMOS technologies a stack of two single devices, serially connected and having a great geometrical distance is not a sufficient condition to suppress totally SETs (see Fig. 6). When the high side MOS is affected by a single event it is unavoidable that an SEE induced current $I_{SEE}$ flows from the drain via the well sheet and contact resistance towards the body contact, even though the corresponding low side MOS maintains its blocking capability. In case that only the low side MOS transistor is affected by a particle strike, there is no failure current at the drain of the corresponding high side MOS, thus avoiding the generation of a SET at the output node. When the SEE induced failure current $I_{SEE}$ produces a sufficiently high voltage drop over the well sheet and contact resistance the corresponding parasitic bipolar transistor will turn on, resulting in a drain failure current due to the short circuit between source drain. With a simple inverter chain test arrangement it is not possible to distinguish between single or multiple SETs events due to charge sharing between adjacent inverters. This means that LET threshold values obtained from inverter chain experiments cannot be simply transferred to more complicated digital circuits such as shift registers built with flip flops which may be much stronger affected by charge sharing effects.

**SET Testing with 126Xe44+ ions**

Heavy ion testing was performed at the RADEF heavy ion accelerator facility at the University of Jyvaskyla, Finland with 126Xe44+ ions having an energy E = 2059 MeV. With a tilt of 0° the linear energy transfer (LET) at the surface is 48.5 MeV $cm^2$/mg@0 µm and at the Bragg peak 69.3 MeV $cm^2$/mg@119 µm. In order to obtain a sufficient energy deposition in the sensitive surface device region the samples were irradiated with a tilt angle of 60° through a 100 µm thick Kapton foil which cause an increase of the LET level and a compression of the LET(x) depth scale resulting in a LET at Bragg peak of 138 MeV $cm^{-2}$/mg@22.5 µm. The chosen particle flux was 1E5 $cm^{-2}$ $s^{-1}$. The samples were exposed to the particle flux for 1000 s giving a fluence of 1E8 $cm^{-2}$. Thus, statistically, one particle strike per 1 $\mu m^2$ is obtained.

Four inverter chain designs were tested with 126Xe44+ ions at a tilt of 60° giving a high LET = 138 MeV $cm^{-2}$/mg@22.5 µm penetrations depth. For a worst case scenario the impact trajectory of the Xe ions in the silicon was adjusted to be in parallel with the gate line of the inverters (see Fig. 1). Thus, more than one transistor in an inverter may be affected by a single event at the same time. As shown in Fig. 7 the four inverter designs D1–D4 differ in the capability of the NMOS and PMOS to reduce the collection of excess minority charge carriers after a particle strike. In all four designs we have used a large vertical distance of 3.7 µm between the single transistors.

Design D1 uses an isolated NMOS with deep n-well formed only in NMOS transistor region. Design D2 uses an NMOS with a deep n-well only in the device region beneath the NMOS ACTIVE, i.e. there is no n-well in the lateral region of the NMOS to form a closed isolating box. In design D3 standard non isolated NMOS were used. Design D4 also employs isolated NMOS as in design D1, but in contrast to design D1 the deep n-well region was extended to the whole inverter area including the PMOS. The deep n-well beneath the PMOS n-well reduces the well sheet resistance, which helps to suppress the turn on of the parasitic PNP bipolar transistor after a particle impact. For the designs D1 and D4 no events were detected at all, i.e. the LET threshold is > 138 MeV $cm^{-2}$/mg. At a LET = 138 MeV $cm^{-2}$/mg the SET cross section $\sigma$ for design D2 was $\sigma$ < 4E−3 $\mu m^2$/inverter and for D3 $\sigma$ < 3E−3 $\mu m^2$/inverter, respectively. The reason for that D2 shows a worse SEE immunity than D3 is due to the fact that the deep n-well beneath the p-well reduces the well sheet resistance in the NMOS which relieves the turn on of the parasitic NPN bipolar transistors after an heavy ion impact. It can be concluded that for standard bulk CMOS inverters with PMOS and NMOS stacks as a hardening by design measure, even at a great distance between the single transistors LET threshold values > 138 MeV $cm^{-2}$/mg cannot be obtained. Only the designs D1 and D4 fabricated in a triple well bulk CMOS process with isolated NMOS reached a target of zero events for LET > 138 MeV $cm^{-2}$/mg.

## 3. Summary

A novel RHBD approach to improve the radiation tolerance of MOS transistors fabricated in a 130 nm bulk CMOS technology in terms of

TID and SET was experimentally verified. To prevent NMOS transistors from TID induced MOS parameter degradations a junction isolation with a distance of the MOS channel from the STI edge $\Delta xj > 0.45$ μm is sufficient. PMOS transistors do not show severe MOS parameter degradations up to a TID of 1.3 Mrad(Si). In contrast to enclosed layout MOS transistors a lateral junction isolation of the MOS channel enables fabrication of MOS transistors with narrow gate widths.

Isolated NMOS enable a reduction of the single event induced additional drain current by reduction of the amount of excess charge carriers which reach the reverse biased drain body diode. The turn on of the parasitic bipolar transistor due to the single event induced additional body currents can be suppressed by a low resistance body connection in the same ACTIVE. The employment of deep n-wells and isolated NMOS together with a low body sheet and contact resistance are essential items to avoid SET generation in digital bulk CMOS circuits.

## Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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