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Towards Uniform Electrochemical Porosification of Bulk HVPE-Grown GaN

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In this paper, we report on results of a systematic study of porous morphologies obtained using anodization of HVPE-grown crystalline GaN wafers in HNO₃, HCl, and NaCl solutions. The anodization-induced nanostructuring is found to proceed in different ways on N- and Ga-faces of polar GaN substrates. Complex pyramidal structures are disclosed and shown to be composed of regions with the degree of porosity modulated along the pyramid surface. Depending on the electrolyte and applied anodization voltage, formation of arrays of pores or nanowires has been evidenced near the N-face of the wafer. By adjusting the anodization voltage, we demonstrate that both current-line oriented pores and crystallographic pores are generated. In contrast to this, porosification of the Ga-face proceeds from some imperfections on the surface and develops in depth up to 50 μm, producing porous matrices with pores oriented perpendicularly to the wafer surface, the thickness of the pore walls being controlled by the applied voltage. The observed peculiarities are explained by different values of the electrical conductivity of the material near the two wafer surfaces.

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Due to excellent properties, which include wide direct bandgap, high thermal stability, high electron mobility and saturation velocity, high sheet carrier concentration at heterojunction interfaces, high breakdown field, low thermal impedance and superior chemical and physical stabilities, gallium nitride (GaN) has become a material of choice for a wide range of applications in optoelectronics and high-power/high-frequency devices, such as light emitting diodes (LEDs) for solid-state lighting¹ and visible light communications (VLC),² laterally diffused metal oxide semiconductor (LDMOS) radio-frequency devices for mobile communication^{3,4} and radar applications.⁵ Besides, high performance characteristics of GaN power devices make them promising for automotive applications.⁶

Nanostructuring of GaN, particularly by using electrochemical (EC) etching, enlarges the areas of applications toward surface enhanced Raman scattering platforms,^{7–10} energy storage,¹¹ photocatalytic,^{12,13} water splitting^{14,15} and hydrogen generation applications,¹⁶ photodetectors,^{17–19} chemical and gas sensors,^{20–24} photonic engineering,^{25–30} waveguides³¹ and Bragg reflectors,^{32–35} and other novel intriguing applications. Note that EC etching is generally a unique approach to micro/nanomachining III-V semiconductor compounds for various purposes.^{36,37}

For many concrete applications it is necessary to integrate a large amount of nanowires in one bundle or array to achieve required functionalities. Over the last decade, different template-based nanofabrication approaches have been developed which offer the possibility to produce large assemblies of nanowires and nanotubes of various materials with defined diameters and lengths. Two types of templates are widely used for nanofabrication purposes, namely porous Al₂O₃^{38–41} and etched ion track membranes based either on inorganic materials or on organic polymers.^{42,43} Both, porous Al₂O₃ and etched ion track membranes, however, exhibit high resistivity and therefore they often play a passive role in nanofabrication processes. In particular, templated growth of nanowires via electroplating is provided usually by the metal contact deposited on the back side of the high-resistivity

membranes, while electroplating of metal nanotubes requires additional technological steps e.g. chemical modification of the inner surface of the pores prior to electrodeposition which leads to the incorporation of spurious phases in the nanotube walls. In this connection an important technological task is the development of cost-effective semiconductor nanotemplates which properties could be easily controlled by external illumination, applied electric fields etc. We have developed a cost-effective technology for controlled fabrication of semiconductor nanotemplates with self-organized quasi-ordered distribution of nanochannels using anodic etching of some III-V (GaAs, InP) and II-VI (CdSe) crystalline substrates in a neutral electrolyte.^{44–46} The high conductivity of the semiconductor nanotemplate skeleton provides conditions for uniform electrochemical deposition of metal species on the inner surface of pores, resulting in the formation of arrays of metal nanotubes embedded in semiconductor matrix.⁴⁴

The electronic band gaps of InP, GaAs and CdSe are 1.3; 1.4 and 1.7 eV at 300 K respectively, which means that the nanotemplates based on these materials are opaque in the visible region of the spectrum. At the same time GaN with the bandgap as high as 3.4 eV at 300 K is feasible for the fabrication of conductive nanotemplates transparent in the whole visible region of the spectrum.

However, despite the expanding applications, the subject of GaN nanostructuring by EC etching still needs better understanding for a wider exploration of novel nanostructures and devices,⁴⁷ especially those requiring porosification in-depth of GaN wafers.

All the produced up to date porous GaN layers are limited to around 2 μm in depth. This is due to fact that, for a long time, GaN has been grown by Metalorganic Chemical Vapor Deposition (MOCVD) on sapphire, Si, or SiC for research and device applications. The thickness of such layers is usually limited to 2–3 μm, and the produced layers suffer from internal strains and defects due to significant mismatches of crystal lattices and thermal expansion coefficients with the substrate material.

Nowadays, there are three main technologies used for GaN bulk crystal growth: hydride vapor phase epitaxy (HVPE), sodium flux and ammonothermal growth.⁴⁸ Among these methods, HVPE growth appears to be the best choice, since the ammonothermal growth seems to be inappropriate for mass production of GaN crystals, providing

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a low growth rate of up to a few micrometers per hour. Apart from that, the properties of ammonothermal GaN crystals are affected by the presence of impurities and other defects that hinder their use for device applications.⁴⁹ On the other hand, the HVPE technology provides relatively high growth rate ($>100 \mu\text{m/h}$) and crystallization of high-purity material.⁴⁸

In spite of important advantages of the HVPE technology, however, achieving a uniform conductivity throughout the bulk material is still challenging since the formation of V-shaped defects or pits leads to the generation of extended inhomogeneities upon subsequent overgrowth [see Ref. 50 and refs therein]. Therefore, deep and homogeneous porosification of HVPE grown GaN wafers is still a challenging issue.

In this paper, we report on elaboration of technological conditions for preparation of porous GaN structures with controlled morphology by anodization of HVPE grown substrates.

Experimental

The experiments have been realized on 2-inch diameter HVPE-grown *n*-GaN single crystalline templates acquired from MTI-CORPORATION - USA. The 300- μm thick wurtzite-phase GaN substrates were of (0001)-orientation. The density of threading dislocations in the substrates was smaller than $1 \times 10^7 \text{ cm}^{-2}$, carrier concentration $>5 \times 10^{17} \text{ cm}^{-2}$ leading to a resistivity $<0.05 \text{ Ohm} \times \text{cm}$. EC etching was carried out in stirred 0.3M HNO_3 , 5% HCl or 3.5M NaCl aqueous solution for 15 min under different voltage biases. An electrical contact was made on the back side of the samples using a conductive silver paste. The anodization of GaN freestanding substrates was carried out in a common two-electrode cell where the sample served as working electrode. A mesh with the surface of 6 cm^2 from platinum wire with 0.5-mm diameter was used as counter electrode. All experiments were performed inside a fume hood at room temperature. A Keithley's Series 2400 Source Measure Unit was used as potentiostat. The morphology of EC-etched GaN samples has been investigated by a Hitachi SU 8230 Scanning Electron Microscope (SEM).

For sample characterization using Scanning Transmission Electron Microscopy (STEM) with a Hitachi HD 2700 instrument, selected specimens were deposited on a standard Cu TEM grid with Formvar and Lacey Carbon polymeric films. In contrast to parallel beam mode (TEM), where only the electrons scattered through the objective aperture placed in the diffraction plane are collected, in convergent beam mode (STEM) the scattered electrons that result after interacting with the sample are collected by a special detector with an annulus around the beam, increasing the signal collection efficiency by sampling more scattered electrons than can pass through an objective aperture. High-resolution scanning transmission electron microscope (HR-STEM) images were digitally processed by using filters in the Fourier space.

Experimental Results and Discussion

The anodic etching of the N-face of the wafer in HNO_3 electrolyte starts with the formation of a porous layer with the thickness around $2 \mu\text{m}$ with most of pores propagating perpendicularly to the wafer surface. Underneath this layer, one can distinguish a complex structure consisting of porous pyramids with dimensions in the range of tens of microns (Fig. 1). These structures disclose the inhomogeneity of electrical conductivity of the wafer near the N-face.

A model has been previously proposed to explain the formation of these three-dimensional self-organized architectures during overgrowth of V-type pits occurring in conditions of variable growth direction.⁵⁰ According to this mechanism, the HVPE growth results in the formation of pyramids consisting of layers with alternating high and low conductivity. The complex structure of each of these pyramids is illustrated in cross-sections (b) and (c) of Fig. 1. One can see the spatial modulation of porosity in pyramids caused by spatial modulation of electrical conductivity. The cross-section of the pyramid marked with asterisk in Fig. 1c reveals highly porous layer separated by totally etched layers in the direction parallel to the pyramid surface. The

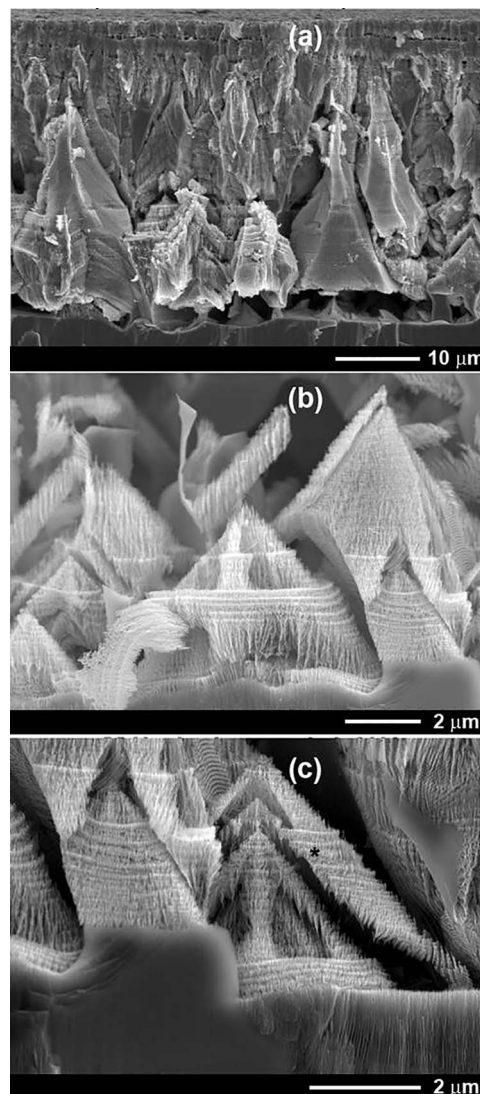


Figure 1. SEM micrographs of porous GaN morphologies produced in depth from the N-face by EC etching in 0.3M HNO_3 electrolyte under 15 V anodic bias: (a) general view of the produced porous layer, and magnified view of pyramids (b, c).

etched layers were of high conductivity, and they were totally etched due to the higher etch rate in high conductivity material.

Different patterns of inhomogeneous electrical parameters in the HVPE grown GaN near the N-face revealed by EC etching are illustrated in Fig. 2. One can observe non-etched regions with low conductivity nearby layered structures (right image), arrays of nanowires formed in regions with high conductivity (left image), and more homogeneous porous regions with pores propagating perpendicularly to the wafer surface (bottom image). The diameter of pores and the pore wall thickness is in the range of 15–25 nm in these regions. This is indicative of the fact that the wafer becomes more homogeneous with increasing the depth from the N-face.

Usually, two types of pores can be generated in semiconductor compounds: current line oriented (CLO) and crystallographically oriented (CO) pores.⁵¹ The characteristics of the pores (shape, velocity of growth, etc.) depend on the specific anodization conditions. It was established that CO pores grow at current densities lower than a certain threshold value, whereas CLO pores grow at current densities higher than the threshold value. The threshold values depend strongly on the free carrier density in semiconductor crystal, electrolyte

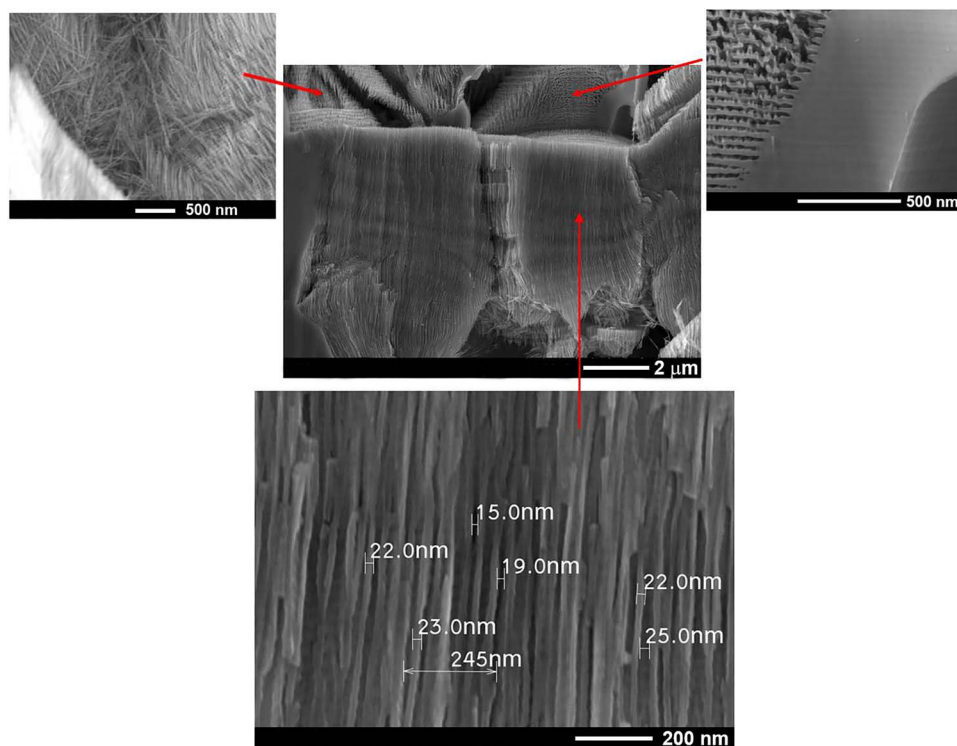


Figure 2. Various nanoporous morphologies obtained at a depth of 40 μm from the N-face upon etching in 0.3M HNO_3 electrolyte.

concentration, and temperature. The main feature of the CO pores is that they grow along definite crystallographic directions.

The influence of the applied anodization voltage on the porosification process is shown in Fig. 3, which presents morphologies obtained with anodization in HNO_3 electrolyte near the N-face. One can see the formation of lamellar structures upon anodization at 18 V (Figs. 3a, 3b) and structures with much smaller degree of porosity obtained under anodization at 10 V, which prove to be more robust and are not destroyed upon sectioning (Fig. 3c), as well as structures containing both CLO and CO pores (Fig. 3d) produced under anodization at 5 V. The formation of crystallographically oriented pores is indicated by their triangular shape in the mid part of Fig. 3d and in the inset. Recently, the influence of the applied anodization voltage upon the shape of pores obtained by lateral anodic etching of MOCVD grown GaN in HNO_3 and NaCl ^{52,53} electrolytes was investigated. It was shown that the cross-sectional shape of pores can be modified from triangular pores to quasi-circular pores with increasing the voltage, which is indicative of the possibility to tailor the shape of pores by design.

Note that the CO pores were observed in other three III-V semiconductors: n-InP, n-GaP and n-GaAs.^{51,54} The main directions of growth for the CO pores in the compounds involved are $\langle 111 \rangle_B$ directions. Another important characteristic of the CO pores is their tendency to self-organized branching along the four $\langle 111 \rangle_B$ directions. It is important to note that the branches can intersect each other.⁵⁵

The electrochemical dissolution behaviors of the N-face GaN in HNO_3 and HCl solutions are characterized by the I–V curves shown in Fig. 3e. Three regions with different slopes can be distinguished in the polarization curves. A very low current level was registered in region I when the applied potential was lower than the breakdown potential or pore formation potential (PFP) equaling 3.5 V. As the potential is increased above 3.5 V, the anodic current first slowly increases, and above about 10 V the current rises steeply. The region II was attributed to the pore formation with low degree of porosity. Further increase in applied voltage (more than 15 V) leads to the formation of pyramidal structures with higher porosity which can be easily destroyed with simultaneous formation of nanowires and

nanowalls (region III). At higher applied biases (more than 20 V) isotropic electrochemical polishing occurs.

The observation that the wafer becomes more homogeneous with increasing the depth from the N-face is corroborated by the analysis of porous morphologies formed nearby the Ga-face of the wafer. The EC etching in HNO_3 electrolyte on the Ga-face of the wafer starts at some nucleation points determined by surface defects and imperfections and proceeds in radial directions at the initial phase of the EC process (see Fig. 4), similar to the process of pore development disclosed previously in GaP.⁵⁶ Usually, the density of the nucleation points (etch pits) depends on the doping concentration of the sample and the applied anodization voltage. The lower is the doping level, the higher is the applied voltage needed for the formation of nucleation points. On the other hand, the higher is the applied voltage at a given doping level of the wafer, the higher is the density of the generated nucleation points. Note that, at a high enough applied voltage, the density of nucleation points will correlate with the density of threading dislocation emerging at the surface of the wafer.

Later-on, the pore growth is dominated by a self-organized process which results in the formation of pores in the direction perpendicular to the wafer surface. The morphology of pores is much more homogeneous as compared to that formed nearby the N-face, which is indicative of a more homogenous electrical conductivity. Porous matrices with pores perpendicular to the wafer surface can be produced at depths larger than 50 μm , as illustrated in Fig. 4a. Apart from that, porous structures with spatially modulated degree of porosity can be obtained by changing the anodization voltage during the pore growth process, see Fig. 4b. It is to be mentioned, however, that the anodization voltage should be increased up to values as high as 100 V to perform porosification nearby the Ga-surface of the wafer. This means that the conductivity of the wafer is much smaller near the Ga-surface as compared to that inherent to the N-face. Taking into account the processing phase diagram for EC etching given in Refs. 25,34,57, one can estimate that the doping concentration is around 10^{19} cm^{-3} near the N-face, and about one order of magnitude smaller near the Ga-face. However, these values are only a rough estimate. Note that the Hall effect measurements would provide information

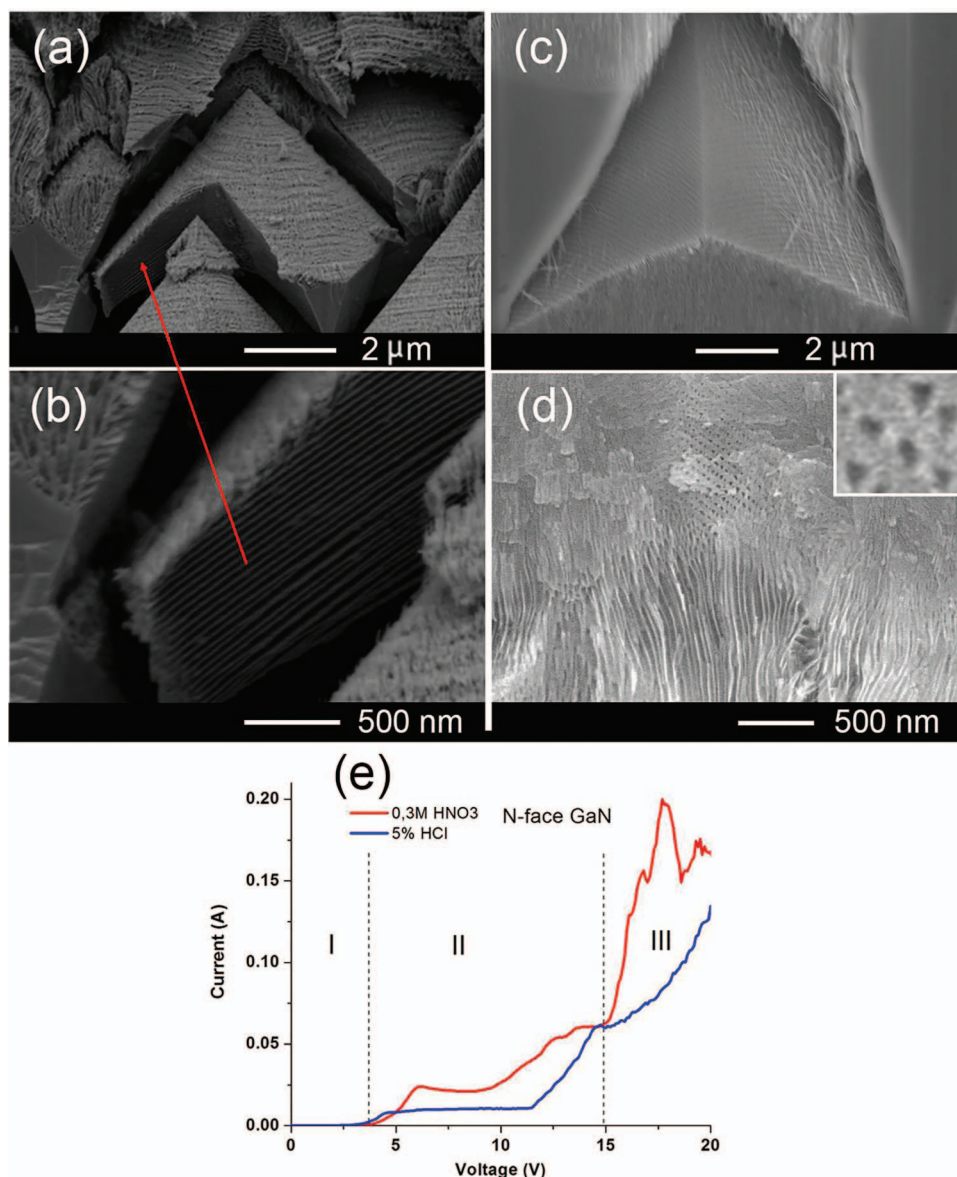


Figure 3. SEM micrographs of porous GaN morphologies produced in depth from the N-surface by EC etching in 0.3M HNO₃ electrolyte under 18 V (a,b), 10 V (c) and 5 V (d) anodic bias. The polarization curves measured at the beginning of the anodization process of GaN on the N-face are shown in (e).

about the integral doping concentration of the free charge carriers over the depth of the wafer.

Figure 5a demonstrates a quite uniform distribution of pores on the surface after removing the nucleation layer, while Fig. 5b shows the pore image in cross-section. Since the depth of pore penetration is high enough, the nucleation layer was removed by a simple cleavage. Mechanical removal was used to avoid the impact of electrolytes during the wet isotropic etching upon the estimation of the diameter of pores and wall thickness.

The diameter of pores and width of the walls is around 60–70 nm. It is to be noted, however, that according to our systematic SEM investigations the ratio of the pore diameter to wall thickness increases with the increase of the anodization voltage. Particularly, the diameter of pores reaches 130 nm when the anodization voltage equals 150 V.

It is believed that highly corrosive, acidic or alkaline etchant such as HF, HNO₃, H₂SO₄ and KOH are indispensable for etching chemically stable GaN. Note that these conventional etchants have many disadvantages, first of all because they are unsafe and environmentally unfriendly. Therefore, one of major challenges for etching GaN

is to search environmentally friendly electrolytes. Schwab et al. recently reported neutral electrolytes such as NaNO₃ and NaCl for etching GaN.⁵⁸ Photoelectrochemical etching of GaN in environmentally friendly ionic liquid electrolytes has been also proposed to address this issue.^{59–61}

We found that HVPE-grown GaN can be efficiently porosified in NaCl electrolyte. Fig. 6a shows a SEM micrograph of the N-surface of the GaN wafer after etching in a 3.5M NaCl electrolyte under 15 V anodic bias. A clear formation of porous circular/hexagonal rings is observed at the surface. Such morphologies with alternation of regions with high and low degrees of porosity are typical for the N-surfaces subjected to EC or photoelectrochemical etching,⁵⁰ and they were attributed to the spatial modulation of the electrical conductivity in the HVPE-grown GaN samples, according to the previously proposed model of HVPE growth. There porous structures develop from the surface to the bulk, as illustrated by a cross-sectional image in Fig. 6b, and the pores penetrate rather deep in the wafer, similarly to the case of etching in the HNO₃ electrolyte, resulting in the generation of pores oriented perpendicularly to the wafer surface in deeper regions exhibiting a more uniform conductivity (Fig. 6c).

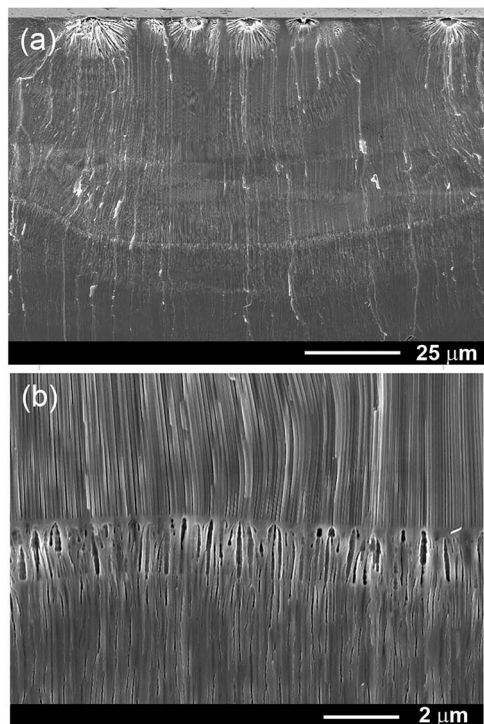


Figure 4. (a) Cross-section SEM micrographs of a porous GaN structure produced in depth from the Ga-face by EC etching in 0.3M HNO₃ electrolyte under 100 V anodic bias. (b) Multilayer porous structure obtained by increasing the applied voltage to 140 V for a short period of time (25 sec) during the EC etching.

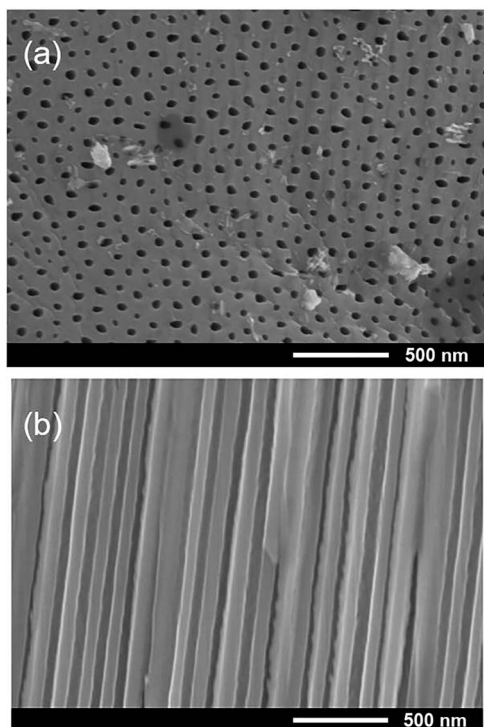


Figure 5. (a) Frontal SEM micrograph of pores produced at the Ga-face by EC etching in 0.3M HNO₃ electrolyte under 100 V anodic bias after removal of the nucleation layer. (b) Cross-sectional SEM micrograph taken after sample porosification.

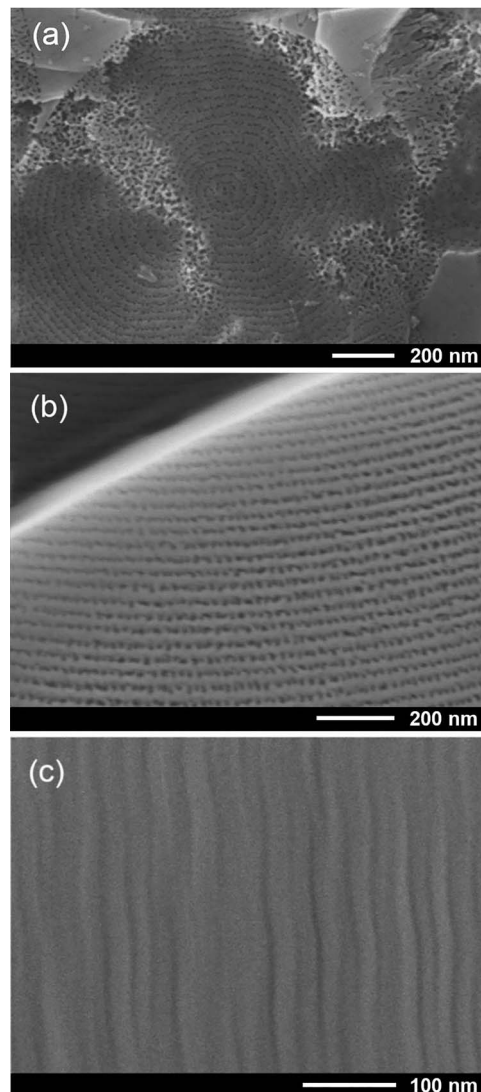


Figure 6. (a) Frontal SEM micrograph of pores produced at the N-face by EC etching in 3.5M NaCl electrolyte under 15 V anodic bias. (b) Cross-sectional view near the N-face. (c) Cross-sectional SEM micrograph of pores in depth from the N-face.

Similar results are obtained with EC etching of GaN wafers in an HCl-based electrolyte, as illustrated by SEM images taken in cross-section in regions situated far enough from the N-face, i. e. in regions with a relatively uniform spatial distribution of the conductivity (Fig. 7). One can see from Fig. 7b the formation of pores with transverse dimensions of 5–10 nm, similar to those produced under EC etching in the NaCl-based electrolyte (Fig. 6c). The similarities in EC etching of GaN in HCl-based and NaCl-based electrolytes may support the suggestion put forward by Zhang et al. concerning the existence of an alternative mechanism of EC etching of GaN,⁵⁹ in addition to the broadly accepted etching mechanism based on semiconductor material oxidation in the EC etching process with subsequent dissolution of the oxide and formation of pores. In case of photo-assisted EC etching of gallium nitride, the predominant intermediate product of the etching process is commonly accepted to be Ga₂O₃ oxide due to the increase of Ga-O bonds on the etched GaN surface.⁶² However, Ga₂O₃ should not be soluble in electrolytes with neutral pH, which is indicative of the existence of another etching reaction for neutral etchants. Taking into account the similarities of etching in HCl and NaCl electrolytes, one may suggest that Cl⁻ plays a major role in the etching process.

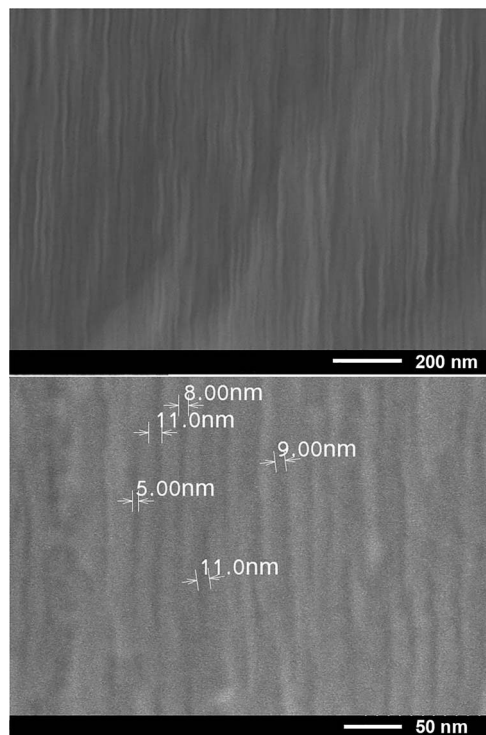


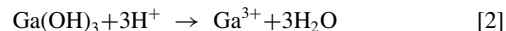
Figure 7. Cross-sectional SEM micrographs of pores produced in depth from the N-face by EC etching in 5% HCl electrolyte under 15 V anodic bias.

The reactions for the formation of porous GaN in HNO_3 electrolyte can be described by Eq. 1 and Eq. 2 representing electrochemical and chemical reactions respectively.⁶³ After the n-GaN crystal is immersed in the electrolyte, an equilibrium of Fermi levels of both materials

results in bending of semiconductor band edges at the junction. The band bending involves the movement of charge carriers from one side of the Schottky junction to another and vice versa. When the potential is applied, and etching voltage is higher than the flatband potential, the electrons will rapidly deplete at the interface and the space charge region (SCR) will form. The generated holes at the GaN/electrolyte interface will participate in the oxidation of the GaN crystal:



Due to the fact that the oxidized product of the GaN is not thermodynamically stable in the acid medium, it will dissolve into Ga^{3+} for further etching of GaN:



Let pass to the discussion of the results of STEM analysis of nanostructures resulting from EC etching of HVPE-grown GaN. Figure 8 shows the STEM images taken in regions similar to those shown in Fig. 2 left, which exhibit arrays of nanowires and fragments of nanowalls. The images were registered using different detectors, namely, secondary electrons (SE) – left, atomic mass contrast (ZC) – middle, and transmission electrons (TE) – right, at the same location on the sample at different magnifications: x100K – first row, x300K – second row, and x700K – third row.

The HR-STEM image acquired in area of the last row in Fig. 8 is shown in Fig. 9. Two lattice spacings between adjacent planes along reciprocal perpendicular directions were found to be of 0.2818 nm and 0.2585 nm. These values correspond to spacing between adjacent (1-100) and (0001) planes of the wurtzite GaN lattice, respectively.^{64,65} The value of 0.2818 nm is larger than the interplanar spacing of stress-free GaN along the [1-100] direction (0.276 nm). It means that the GaN nanowire lattice is strained in this direction, and the estimated strain value is around 2%. Note that a similar strain value along this crystallographic direction was found in porous GaN structures produced by EC etching in a NaNO_3 solution.⁶⁶

An important observation from Figs. 9d, 9e is that the angle between the [1000] and [1-100] directions differs by 2° from 90° .

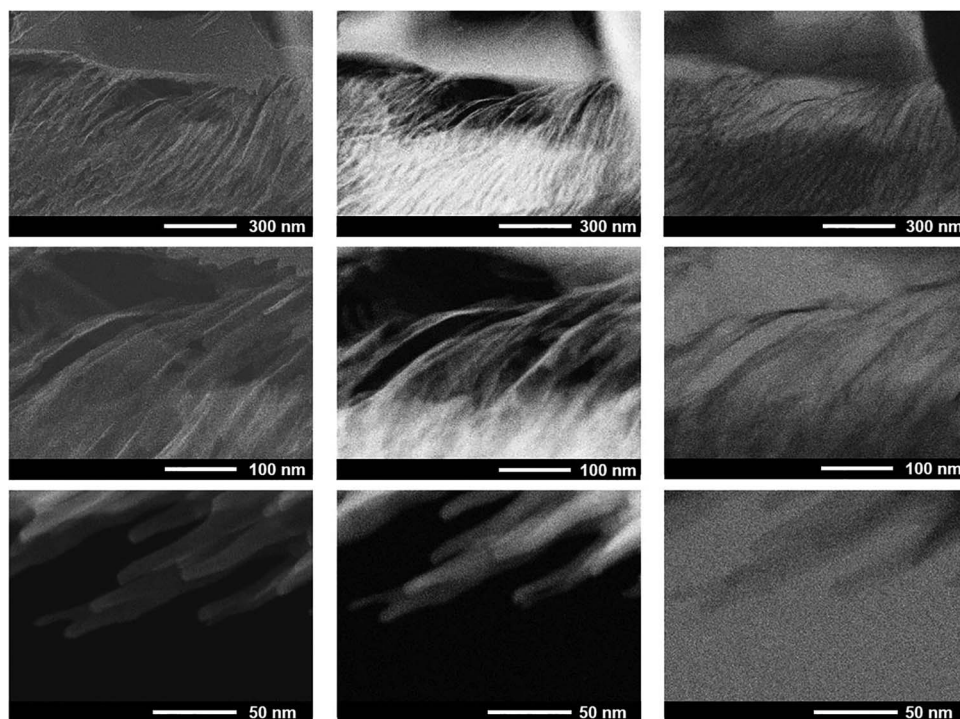


Figure 8. STEM micrographs of GaN nanostructures resulting from EC etching. Different detectors were used: secondary electrons (SE) – left, atomic mass contrast (ZC) – middle, and transmission electrons (TE) – right, at the same location on the sample at different magnifications: x100K – first row, x300K – second row, and x700K – third row.

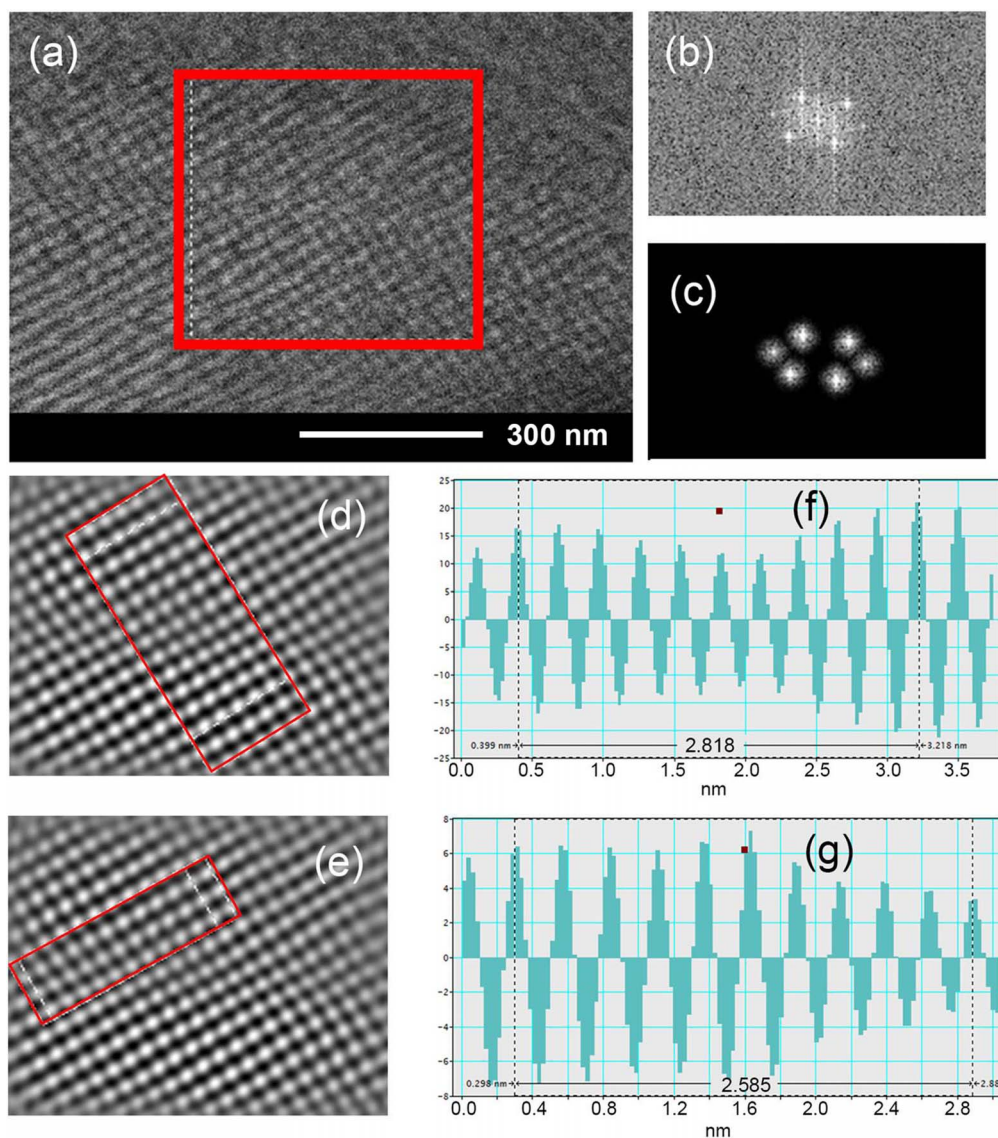


Figure 9. HR-STEM analysis of a GaN nanowire produced with EC etching. (a) Area chosen to perform d-spacing measurements. (b) FFT filtered image from selected area. (c) Applied mask on the FFT filtered image from the selected area. (d, e) Inverse FFT images extracted from the FFT filtered image in the selected area. (f, g) Profiles obtained from the marked area in the inverse FFT image.

Nevertheless, the investigations demonstrate that the grown GaN wafer is single crystalline as a whole. Therefore, the revealed by EC etching inhomogeneities are related to spatial modulation of the electrical conductivity of the material rather than to crystal structure inhomogeneity. This is an encouraging finding which is indicative of the prospects of producing homogeneous porous structures over the entire HVPE-grown wafer, providing that the issues of reducing the modulation of doping during the crystal growth are properly addressed, particularly by avoiding the formation of V-type pits in the growth process. The feasibility of uniform porosification of bulk GaN is demonstrated by the production of deep enough homogeneous porosity near the Ga-face of the HVPE-grown wafer.

Conclusions

The results of this study disclose different porous morphologies produced by EC etching in the depth of a HVPE-grown wafer with respect to the N- or Ga-face. Complex porous pyramidal-type structures are formed at a depth of several tens of micrometers from the N-face, while homogenous porous matrices with pores oriented perpendicular to the wafer surface are generated at a depth of up to 50 μm at the

Ga-face. These features are explained by variations in the electrical conductivity across the wafer resulting from the mechanisms of the HVPE growth. Possibilities of producing porous structures in environmentally friendly electrolytes of the NaCl-type are demonstrated. The comparison of porous morphologies with those obtained under anodization in HCl electrolytes suggests the existence of an alternative mechanism of EC GaN etching, in addition to the broadly accepted etching mechanism involving the formation of a Ga_2O_3 oxide as an intermediate product of the EC etching. The HR-STEM analysis of the produced GaN porous structure demonstrates the preservation of the good wurtzite-type crystalline phase of the material. The obtained results pave the way for wafer-scale nanoporous GaN production for various optical, optoelectronic and photonic applications.

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