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To cite this article: M Elattar et al 2020 Semicond. Sci. Technol. 35 095011

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Semicond. Sci. Technol. 35 (2020) 095011 (11pp)

High-brightness broad-area diode lasers with enhanced self-aligned lateral structure

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Received 6 March 2020, revised 25 May 2020 Accepted for publication 11 June 2020 Published 27 July 2020



Abstract

Broad-area diode lasers with increased brightness and efficiency are presented, which are fabricated using an enhanced self-aligned lateral structure by means of a two-step epitaxial growth process with an intermediate etching step. In this structure, current-blocking layers in the device edges ensure current confinement under the central stripe, which can limit the detrimental effects of current spreading and lateral carrier accumulation on beam quality. It also minimizes losses at stripe edges, thus lowering the lasing threshold and increasing conversion efficiency, while maintaining high polarization purity. In the first realization of this structure, the current block is integrated within an extreme-triple-asymmetric epitaxial design with a thin p-doped side, meaning that the distance between the current block and the active zone can be minimized without added process complexity. Using this configuration, enhanced self-aligned structure devices with 90 μ m stripe width and 4 mm resonator length show up to 20% lower threshold current, 21% narrower beam waist, and slightly higher (1.03×) peak efficiency in comparison to reference devices with the same dimensions, while slope, divergence angle and polarization purity remain almost unchanged. These results correspond to an increase in brightness by up to 25%, and measurement results of devices with varying stripe widths follow the same trend.

Keywords: broad-area diode laser, self-aligned structure, two-step epitaxial growth, current block, current confinement, beam quality, brightness

1. Introduction

High-power broad-area diode lasers (BALs) based on GaAs offer the highest power-conversion efficiency η_E among all light sources. η_E is defined as the ratio of optical output power P_{opt} to electric input power $P_{el} = I \cdot U$, where I and U are the operating current and voltage respectively. As a result, BALs

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are used in a wide range of applications, including industrial and space applications, where enhancement of η_E is highly beneficial and commercially valuable [1].

Many high-power applications also require high beam quality for efficient coupling into an optical fiber or any given optical system. In a typical high-power BAL, the output beam is close to the ideal case of a diffraction-limited profile in the vertical (fast) axis, while in the lateral (slow) axis, the profile strongly deviates from the diffraction-limited case, corresponding to lower beam quality. It is thus important to improve lateral beam quality, which is quantified here using the lateral beam parameter product $BPP_{\text{lat}} = \frac{1}{4} \times w_{95\%} \times \theta_{\ell,95\%}$, where $w_{95\%}$ and $\theta_{\ell,95\%}$ are respectively the lateral near-field width and far-field angle with 95% of the total power content. High-brightness BALs exhibit low BPP_{lat}

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at high P_{opt} , where (lateral) brightness is parametrized as $B_{lat} = P_{opt}/BPP_{lat}$. Achieving high brightness in BALs is highly beneficial for their use in direct applications or as pump sources for solid-state and fiber lasers [2]. Another important performance metric of BALs is polarization purity, which is quantified here using the degree of polarization DOP = $P_{TE}/(P_{TE} + P_{TM})$, where P_{TE} and P_{TM} are the TE- and TM-polarized output power, respectively [3]. High DOP allows highly-efficient polarization beam combining (PBC), which is used in many systems to increase P_{opt} of BALs [4, 5].

It has been discussed in previous work [6-8] that in addition to thermal lensing, there are non-thermal mechanisms that can have significant detrimental effects on beam quality, namely lateral current spreading and lateral carrier accumulation (LCA) at stripe edges. Reducing current and carrier density at stripe edges results in lower gain for higher-order lateral modes, and can even reduce the number of guided modes. This can lead to smaller $w_{95\%}$ and $\theta_{\ell,95\%}$, and thus lower BPP_{lat} . Many lateral structuring techniques have been developed to realize this central confinement of current and carriers in GaAs-based BALs, where the challenge is to enhance beam quality without compromising $\eta_{\rm E}$, maximum $P_{\rm opt}$, or device lifetime. One of these techniques is high-energy deep ion implantation to prevent current flow in the device edges. Implantation profiles that reach the n-doped side of the BAL, i.e. through the active zone, eliminate current spreading in the p-side and suppress LCA due to the rapid recombination of carriers that diffuse into the device edges at the point defects introduced by implantation. This results in reduced $w_{95\%}$ (10%) and $\theta_{\ell,95\%}$ (27%), but $\eta_{\rm E}$ and maximum $P_{\rm opt}$ are strongly compromised [8]. A tailored implantation profile, with the implant halted above the active zone, has demonstrated a significant reduction of BPP_{lat} with minimal reduction of $\eta_{\rm E}$ [9]. Deep-etched index-guiding trenches also confine carriers to the device center, resulting in increased $\eta_{\rm E}$, but they introduce a large index step that reduces beam quality and strain fields that decrease DOP [3].

Other lateral structuring techniques for central confinement of current and carriers have also been demonstrated, which are based on two-step epitaxial growth processes. One such technique is the real-index guided self-aligned structure (RISAS), which was developed to enhance the performance of single-mode high-power lasers and overcome the limitations of ridge waveguide diode lasers [10, 11]. In this structure, a sequence of layers, one of which is n-doped, are grown within the p-doped waveguide layer of the diode laser, resulting in a current-blocking reverse-biased junction in close proximity to the active zone. An intermediate etch step between two growth stages removes the n-doped layer from the central stripe, and since the n-doped layer is designed to have a lower refractive index than the regrown layers, the final structure exhibits lateral index guiding and current confinement. Despite the complex growth process, RISAS diode lasers have demonstrated low threshold current ($I_{\rm th}$) and high $\eta_{\rm E}$ and $P_{\rm opt}$ at a resonator length (L) of 1.6 mm and stripe widths (W) varying between 3 and 50 μ m. However, the strong lateral index guiding in the RISAS would significantly increase BPP_{lat}, making it unsuitable for realizing high-brightness BALs. The buried mesa structure (BM) is another confinement technique that has been implemented in BALs, in which the quantum well (QW) is etched outside of the central stripe between two growth stages [12]. In this structure, there is no true barrier to lateral current spreading, but carriers in the QW are still confined to the device center by lateral energy barriers that are created upon epitaxial regrowth, due to the higher band-gap energy of the regrown (waveguide) layers in comparison to the QW. This band-gap energy difference also leads to a lateral refractive index step, resulting in built-in index guiding. In comparison to standard BALs, BM devices ($W = 100 \ \mu m$, L = 4 mm) have demonstrated lower I_{th} (12–16%) and higher slope (8–11%), resulting in higher $\eta_{\rm E}$ and $P_{\rm opt}$, while maintaining high DOP. On the other hand, BPP_{lat} was higher in BM devices, as a result of the broader near-field width and far-field angle. This is a consequence of the aforementioned index step which allows the guiding of a larger number of higher-order lateral modes, thus resulting in lower beam quality and limiting the brightness achievable by the BM structure. A further confinement technique in BALs is the lateral buried implantation (LBI) structure, in which a buried current aperture is created by implanting heavy ions, such as O^+ or Si⁺, outside of the central stripe between two growth stages [13, 14]. Although epitaxial regrowth acts as an annealing step which removes most of the lattice defects caused by ion implantation, the implanted regions still block current flow because the heavy ions introduce deep and shallow levels in the band gap, which either compensate doping and create a reverse-biased junction, or shift the pn-junction away from the QW, resulting in an insulation effect. In one realization of LBI BALs, they have demonstrated lower $I_{\rm th}$ (4-12%) and higher slope (11-15%) in comparison to standard BALs ($W = 100 \ \mu m$, $L = 4 \ mm$). Their BPP_{lat} values were lower than standard BALs, but the difference was relatively small. In another realization, where the current aperture was located very close to the active zone, BPP_{lat} was more strongly reduced, but $\eta_{\rm E}$ was also reduced, likely due to contamination or other interface defects at the regrowth interface, as well as implant-generated non-radiative recombination centers.

In this work, we develop an enhanced variant of another lateral structure which also operates by current confinement to the device center to reduce current spreading and LCA at stripe edges, namely the self-aligned structure (SAS). This structure is based on a two-step epitaxial growth process with an intermediate etching step, and previous research has shown its potential to simultaneously achieve high η_E , low *BPP*_{lat} and high DOP at high values of P_{opt} [5, 15–17]. The enhanced variant presented here shall be referred to as 'eSAS', and is expected to have significant advantages over established SAS designs and other aforementioned techniques. A schematic of an eSAS diode laser is shown in figure 1, with a detailed description of the implemented configuration and potential advantages in section 2.



Figure 1. Schematic of the final configuration of a diode laser chip with enhanced self-aligned lateral structure (eSAS) after the two-step epitaxial growth sequence, showing the position of the current-blocking layers within the structure as well as their thicknesses and doping concentrations.

2. Chip design and simulation results

2.1. Vertical structure

For this realization, an extreme-triple-asymmetric (ETAS) epitaxial design is selected, which is designed to operate at a wavelength $\lambda \approx 940$ nm. The design process is described in detail in [18, 19]. The design has a thin p-doped side, consisting of the following layers (in growth order): a very thin lightly-doped AlGaAs waveguide layer with low Al content, a moderately-doped AlGaAs cladding layer with high Al content, a highly-doped GaAs sub-contact layer, and finally a thin very-highly-doped GaAs contact layer upon which the contact metallization is subsequently deposited. It is designed for single vertical mode operation, i.e. the fundamental mode (mode 0), following standard techniques. The fundamental mode is strongly shifted towards the n-doped side of the diode as a result of the thin waveguide and the high Al content of the cladding, and the relative thicknesses of the graded-index transition layers on both sides of the QW are used to shape the modal profile and control the optical confinement factor (Γ). Since the optical field extends only minimally into the p-side cladding layer, the thickness of this low-mobility layer is minimized to reduce electrical resistance, resulting in a combined thickness < 800 nm for the cladding and waveguide layers. However, sufficient p-side thickness must be maintained, to protect the active zone from mechanical damage or stresses that can be induced during processing, handling or soldering. This is achieved here by including a thick high-mobility GaAs sub-contact layer, similar to previous publications [14].

By optimizing the thickness, composition, and doping concentration of each of the aforementioned layers, the ETAS design enables combining low optical loss α_i and series resistance R_s with high Γ to obtain low I_{th} , high η_E and reduced thermal power saturation. The ETAS variant used in this work has $\Gamma \approx 1\%$, $\alpha_i \approx 0.5 \text{ cm}^{-1}$, and a vertical far-field angle (95% power content) $\theta_{v,95\%} \approx 67.7^{\circ}$.

2.2. Lateral configuration and fabrication process

The eSAS is implemented as the lateral configuration of the diode laser chips, as mentioned in section 1. In this structure, a two-step epitaxial growth sequence is used to introduce current blocks in the device edges, i.e. outside the laser stripe, thus confining current flow to the center. This is achieved by growing n-doped layers within one of the layers of the p-side of the diode, thus creating a reverse-biased junction that prevents current flow. The epitaxy is paused after growing these current-blocking layers to carry out an intermediate lateral structuring step, where the n-doped layers are selectively etched exclusively in the device center, thus creating a current aperture. The remaining p-side layers are finally regrown over the structured surface, resulting in the final chip configuration in figure 1.

This structure has some advantages over the different lateral structuring techniques described in section 1, which can allow it to achieve better overall performance. For example, highenergy deep ion implanation generates point defects, which can result in higher carrier loss and reduced slope [8]. It is also challenging to precisely control the implantation depth and damage profile due to the stochastic nature of implantation, with typical profiles spreading over hundreds of nanometres [20]. The BM structure in [12] has a built-in lateral refractive index guide, which allows the guiding of a larger number of higher-order lateral modes, and therefore leads to lower beam quality. The LBI structure in [13, 14] is similar to the eSAS, but with a heavy-ion implantation step instead of the intermediate etching step. LBI structures have demonstrated improved threshold, slope and beam quality compared to standard BALs, but a significant enhancement of beam quality could so far only be obtained by compromising conversion efficiency. As previously mentioned, a precise definition of the implantation profile, and thus the location of the current block, can also be challenging in LBI structures.

As discussed in section 1, the SAS has demonstrated improvements in efficiency, beam quality and polarization purity of BALs [5, 15–17]. In contrast to implantation-based lateral structuring techniques, current blocking in the SAS is realized using epitaxial layers, whose location, thicknesses and doping concentrations can be precisely defined for a given design. In this work, the eSAS is presented as an optimized variant of previous SAS realizations, that can overcome their limitations and simultaneously enhance all aspects of BAL performance. For example, the n-doped materials used to grow the current-blocking layers are changed, resulting in higher precision of the etching depth and thus higher process control and repeatability, as well as stronger current blocking. In addition, by integrating the blocking layers within the aforementioned ETAS vertical design, they can be grown closer to the active zone than in previous realizations without added process complexity, resulting in stronger reduction of current spreading. The eSAS design process and its advantages over previous SAS realizations are described in detail in the next section.

2.3. Setting design parameters

The eSAS offers several degrees of design freedom, namely the vertical position, materials, thicknesses, and doping concentrations of the blocking layers. For the first realization, the layers are placed near the bottom of the GaAs subcontact layer, as shown in figure 1. Placing the layers within a GaAs layer allows the intermediate etching step to be performed ex-situ, i.e. outside the MOVPE (metalorganic vapour-phase epitaxy) reactor. If the layers had been placed deeper within the pside, i.e. within AlGaAs layers, the etching step would have to be performed in-situ to prevent the oxidation of the exposed aluminum, making it a significantly more complex process. Within the grown ETAS epitaxial design (see section 2.1), placing the blocking layers near the bottom of the subcontact layer means that they are roughly half way between the p-side surface and the active zone, thus preventing current spreading within the top half of the p-side of the diode. This highlights the benefit of selecting this ETAS design for realizing the eSAS: the p-side waveguide and cladding layers (both made of AlGaAs) have a combined thickness < 800 nm, meaning that the blocking layers can be placed relatively close to the active zone without the added complexity of etching and regrowth at an AlGaAs interface. This is a significant improvement over previous SAS realizations, in which the cladding layer on its own had a thickness of 1 μ m [17].

The current blocking is realized using two n-doped layers: a GaAs layer on top of an InGaP layer, as opposed to only GaAs in previous realizations [5, 15–17]. This realization allows selective patterning using wet chemical etching; the InGaP acts as an etch-stop layer for the etching solution of GaAs and

vice versa, as described in [12], thus enabling the definition of the etching depth with high precision. In order to set the design parameters of the two blocking layers, namely thicknesses and doping concentrations, simulations are carried out using the 'WIAS-TeSCA' simulation tool [21], based on solving the one-dimensional drift-diffusion equation to estimate the current-voltage (I-U) characteristics, with the results shown in figure 2. The leftmost graph demonstrates an additional benefit of including the InGaP blocking layer, as opposed to a current block made of only GaAs, namely that InGaP has a higher bandgap energy than GaAs, and therefore enhances current blocking. However, replacing the 20 nm InGaP layer by GaAs only reduces the turn-on voltage by 0.2V. It is thus clear that the influence of InGaP on current blocking is relatively small, but as previously mentioned, its main benefit is allowing the precise definition of the etching depth. The middle graph shows a decrease of the turn-on voltage by 4.5 V upon decreasing the total thickness of the blocking layers (d_{block}) from 60 to 30 nm, while maintaining a 2:1 ratio between the thicknesses of GaAs and InGaP (d_{n-GaAs} and $d_{n-InGaP}$, respectively). The rightmost graph shows a decrease by 4.1 V upon decreasing the doping concentration of the blocking layers $(N_{D,block})$ from 2×10^{18} to 1×10^{18} cm⁻³. These results demonstrate that increasing thicknesses and doping concentrations of the blocking layers results in enhanced current blocking. However, limits have to be set for these parameters in our design. Thicker blocking layers result in lower mechanical flatness of the device surface after regrowth, which can induce strain and reduce the polarization purity of the laser emission [5]. The doping concentration of the n-doped blocking layers cannot easily be increased beyond (4-5) $\times 10^{18}$ cm⁻³, because the silicon dopant tends to self-compensate or form precipitates at high concentrations [22], which can result in device failure. With these considerations in mind, the following baseline configuration is chosen for the blocking layers (see figure 1): $d_{\text{block}} = 60 \text{ nm}$, with $d_{\text{n-GaAs}} = 40 \text{ nm}$ and $d_{\text{n-InGaP}} = 20 \text{ nm}$, and $N_{\text{D,block}} = 2 \times 10^{18} \text{ cm}^{-3}$ for both layers. The simulation estimates a very high turn-on voltage for the resulting p-n-p blocking structure (~7.3 V for 1 A/cm² current density, see figure 2), far beyond the voltage range of a BAL, which means that this structure is expected to reliably block current throughout high-power operation.

It is important to determine if a lateral index guide is introduced by adding the blocking layers in the device edges, because an index guide would result in stronger mode guiding in the laser stripe, a larger number of higher-order lateral modes, and therefore lower beam quality. Using an in-house waveguide equation solver called 'QIP2' [23], the guided vertical modes are simulated in the central injection region and the outer blocking region of the device, based on the refractive index profile of the grown layer structure. Figure 3 shows the refractive index profile and the resulting intensity profile of the fundamental vertical lasing mode (mode 0, see section 2.1). In each region, the effective refractive index of mode 0 $(n_{\text{eff},0})$ is determined, and the difference in $n_{\rm eff,0}$ between the central and outer regions ($\Delta n_{\rm eff,0}$) is then a metric for the lateral index step that results in waveguiding. Despite the InGaP layer having a lower refractive index than the GaAs surrounding it,



Figure 2. Simulated current density as a function of voltage in one-dimensional structures incorporating current-blocking layers. The baseline blocking configuration (see figure 1) is compared to configurations with no InGaP (left), with half the thickness of the blocking layers (middle), and with half their doping concentration (right).



Figure 3. Refractive index and normalized optical intensity of the fundamental vertical lasing mode as functions of vertical position along the layer structure in the central injection region (left) and the outer blocking region (right) of an eSAS diode laser.

 $n_{\rm eff,0}$ remains identical in the central and outer regions, i.e. $\Delta n_{\rm eff,0} = 0$, meaning that the InGaP layer has no effect on lateral waveguiding. This is another benefit of using the ETAS design, where mode 0 is strongly shifted towards the n-doped side of the diode (see figure 3) and therefore far removed from the InGaP layer, which as a result has practically no effect on its $n_{\rm eff}$ value.

2.4. Simulating performance of enhanced self-aligned structure diode lasers

To get an estimate of the effectiveness of the eSAS in reducing lateral current spreading and thus improving laser performance, two further simulations are carried out. First, we follow the analytical approach described in [24, 25] to simulate current spreading at lasing threshold in devices with stripe width $W = 90 \ \mu m$ and resonator length $L = 4 \ mm$. In this approach, the lateral current density profile within the active zone is approximated by assuming constant current density under the stripe, which is set here to the threshold current density (J_{th}), calculated as described in [19]. It also assumes that the active zone is very thin, and that the residual layer thickness below the current block, in which current spreads, is small in comparison to W. Figure 4(a) compares the simulated profiles of eSAS devices, reference devices without the current block, as well as the ideal case of current injection with no spreading. It clearly shows the strong reduction in current spreading by introducing the current block. From the current density profiles, the threshold current $I_{\rm th}$ is calculated in each case, and the values are shown in figure 4(b). In comparison to the ideal injection case, the reference device is estimated to have a 45% higher Ith, compared to 15.5% for the eSAS device, which corresponds to a 65.5% reduction of current loss at device edges by implementing the eSAS. This indicates that $I_{\rm th}$ is expected to strongly decrease in the eSAS structure, because by reducing current spreading to the edges, the threshold current density can be reached under the stripe at a lower total current.

In the second simulation, WIAS-TeSCA [21] is used to numerically solve (self-consistently) the two-dimensional drift-diffusion equations, the optical Helmholtz equation, and the rate equation for the optical power, assuming spatial homogeneity in the longitudinal direction. The lateral current and



Figure 4. Simulation results based on the analytical approach in [24, 25], comparing the eSAS to the reference (no current blocking) and ideal injection (no current spreading) cases in terms of: (a) current density at lasing threshold within the active zone as a function of lateral position, and (b) threshold current I_{th} in each case.



Figure 5. WIAS-TeSCA simulation results comparing eSAS and reference devices (stripe width $W = 20 \mu m$, single lateral mode) in terms of lateral current density and optical intensity as functions of lateral position at (a) I_{th} and (b) 5A, as well as (c) voltage, optical power and conversion efficiency as functions of current.

carrier density profiles and the power-voltage-current (PUI) characteristics are thus accurately calculated. The simulation is carried out on one half of symmetric $W = 20 \ \mu m$ devices, and is simplified by taking a single strongly-index-guided lateral mode into consideration to exclude carrier-densitydependent lateral waveguide effects. The simulated lateral current density profiles are shown in figures 5(a) and (b) for reference and eSAS structures biased at Ith and 5A respectively, showing in both cases a strong reduction in current spreading. In each case, the normalized optical intensity profile of the lateral mode is also shown, which is identical in both structures. Upon increasing the current from $I_{\rm th}$ to 5A, the full width at half maximum (FWHM) of the lateral mode is reduced from 11.8 to 9.9 μ m. Figure 5(c) compares the estimated PUI characteristics of the two devices. The eSAS device shows lower $I_{\rm th}$ and increased slope, which result from the reduced current spreading. It also shows increased R_s represented by the higher slope of the voltage-current (U-I) curve, which is due to the confinement of current to a smaller area. The overall result is an increase in $\eta_{\rm E}$, in spite of the higher voltage. The simulation of a narrow stripe width device with a single lateral guided mode makes this a sensitive test compared to practical broad-area diode lasers, resulting in exaggerated performance differences which are not expected in practice. However, it is useful to qualitatively estimate the effects of reduced current spreading in the eSAS on laser operation, since the analytical model is limited to simulating the current density distribution at lasing threshold and estimating I_{th} .

3. First realization and measurement results

3.1. Process content and quality testing

As a first step towards the realization of eSAS diode lasers, epitaxial wafers are grown using metalorganic vapour-phase epitaxy (MOVPE). As described in section 2, the growth is carried out in two steps, with an intermediate ex-situ wet chemical etching step that selectively removes the currentblocking layers in the device center to create a current aperture. In the first realization of the eSAS diode lasers, each epitaxial wafer is processed to include several single-emitter (SE) variants, in addition to a few devices that do not undergo the intermediate etching step. These unetched devices are thus simple blocking structures which cannot be operated as



Figure 6. Measured current density as a function of voltage, comparing the current-blocking capability of: (a) structures with varying block thicknesses d_{block} at a constant heat-sink temperature $T_{HS} = 25^{\circ}$ C, and (b) the baseline structure with $d_{block} = 60$ nm at varying T_{HS} .



Figure 7. SEM images of an eSAS diode laser after the two-step epitaxial growth sequence, shown relative to their position on a schematic. The left image, produced using a back-scattered electron (BSE) detector, highlights the interface between the injection and blocking regions as well as the active zone, while the right image, produced using a secondary electron (SE) detector, gives a clearer view of the interface and the blocking structure.

lasers because the blocking layers prevent current from flowing through the device. These devices are included to measure their I-U characteristics and test the effectiveness of the current block we have included in our design. Figure 6(a) shows the I-U characteristics of current-blocking devices with $d_{block} = 60$ and 30 nm, in comparison to an etched non-blocking device. The 60 nm variant corresponds to the baseline configuration (see section 2.3) with $d_{n-GaAs} = 40$ nm, $d_{n-InGaP} = 20$ nm, and $N_{\text{D,block}} = 2 \times 10^{18} \text{ cm}^{-3}$. The 30 nm variant maintains the same $N_{\text{D,block}}$, while $d_{\text{n-GaAs}}$ and $d_{\text{n-InGaP}}$ are reduced to 20 and 10 nm, respectively. All measured devices have W = 90 μ m and L = 2 mm, and their I-U characteristics are measured using a single probe needle connected to a source-measure unit (SMU) that simultaneously supplies voltage and measures current. As indicated on figure 6(a), the effectiveness of each block variant is quantified by comparing the current density that flows through it at the voltage $(U_{\rm th})$ corresponding to $J_{\rm th}$ in the non-blocking device, where J_{th} is calculated as described in [19]. At $U_{\rm th}$, the 30 nm variant allows a current density of $\sim 0.25 \times J_{\text{th}}$ to flow, indicating that its blocking capability may be insufficient. On the other hand, the current density at U_{th} in the 60 nm variant is lower than 0.001% of J_{th} , and only reaches a significant current level (1% of J_{th}) at ~0.9 V above U_{th} . Even at higher heat-sink temperatures (T_{HS}) up to 65°C, this variant reliably blocks current, with the current density reaching 1% of J_{th} at ~0.7 V above U_{th} , as shown in figure 6(b). Simulations predicted significantly higher currentblocking capability from the 60 nm variant (see figure 2), which remains a topic for further investigation. Nevertheless, the measurement results still clearly demonstrate that this variant, which we have chosen as a baseline, provides adequate blocking for the realization of eSAS BALs.

All SE variants are processed to have L = 4 mm. In the eSAS devices, W is defined by the width of the etched aperture in the center of the current block W_{ap} , which varies in the following range in the implemented process: 20, 50, 90, and 186 μ m. In addition, reference devices are processed following standard techniques on the same wafer, in which the blocking layers are completely etched. In these devices, W is defined by a shallow implant which limits current injection in the p-doped contact layer to a window with a defined width W_{imp} , which has the same aforementioned range of values of W_{ap} .



Figure 8. Measurement results comparing exemplary reference and eSAS single-emitters with stripe width $W = 90 \ \mu\text{m}$ and resonator length $L = 4 \ \text{mm}$ in terms of: voltage, optical power P_{opt} and conversion efficiency η_{E} as functions of current (top-left), lateral beam parameter product *BPP*_{lat} as a function of P_{opt} (top-right), as well as normalized optical intensity as a function of lateral near-field position (bottom-left) and far-field angle (bottom-right) at $P_{\text{opt}} = 10 \ \text{W}$.

By processing eSAS and reference devices on the same wafer, a fair comparison can be made to determine the benefits and drawbacks of the eSAS.

When the process is completed, scanning-electronmicroscope (SEM) images of processed devices are taken to verify that the design has been correctly implemented. Examples of these SEM images are shown in figure 7, with no indication of epitaxial, etch or process defects. The wafers are cleaved into bars, each having a variety of SEs, and their facets are passivated by ZnSe and then coated with dielectric layers, such that the reflectivities of the front and rear mirrors are 1% and 98% respectively. The bars are then cleaved into individual SE chips, which are then mounted p-side down on copper-tungsten (CuW) submounts for effective heat spreading and minimization of the thermal resistance $R_{\rm th}$, which is typically in the 2-3 K/W range. Each mounted SE chip is then tested by measuring its PUI characteristics, DOP, and near-field and far-field profiles of its output beam, where all measurements are carried out under continuous-wave (CW) operation at 25°C, with the temperature sensor positioned at the rear edge of the submount. The measurement of the PUI characteristics uses a four-terminal configuration to accurately measure the voltage across the chip, and the optical output power is measured using a calibrated thermoelectric detector, while the near-field and far-field beam profile measurements use a telescopic arrangement to image the profiles onto a moving slit. The measurement techniques are described in more detail in [3].

3.2. Analysis of measurement results

The measurement results of exemplary eSAS and reference SEs with $W = 90 \ \mu m$ are shown in figure 8. The performance of the two devices is compared in terms of PUI characteristics, BPP_{lat} at varying P_{opt} , as well as lateral near-field and far-field intensity profiles at $P_{\text{opt}} = 10$ W. Key performance metrics of exemplary eSAS and reference SEs with varying W = 50, 90 and 186 μm are reported in table 1, including metrics extracted from PUI characteristics (I_{th} , slope and η_{peak}), as well as beam quality metrics ($w_{95\%}$, $\theta_{\ell,95\%}$ and BPP_{lat}) and DOP at optical operation powers P_{op} that vary with W.

In terms of PUI characteristics, eSAS devices show strongly reduced I_{th} , which is in agreement with the predicted trend from the simulations (see figures 4 and 5). The measured slope values in eSAS and reference devices are very similar, lying within the $\pm 1.5\%$ error margin reported in [1]. A detailed

W(µm) / Structure	<i>I</i> _{th} (mA)	Slope (W/A)	$\eta_{ m peak}$ (%)	P _{op} (W)	_{W95%} (μm)	θ _{ℓ,95%} (°)	BPP _{lat} (mm∙mrad)	$\frac{B_{\text{lat}}}{(W/(\text{mm}\cdot\text{mrad}))}$	DOP (%)
50/reference	474	1.08	64.1	5.0	66.68	6.55	1.91	2.62	99.2
50/eSAS	321	1.07	64.8		58.06	6.19	1.57	3.19	99.5
90/reference	613	1.08	64.8	10.0	98.65	9.48	4.08	2.45	99.2
90/eSAS	489	1.08	66.5		77.63	9.63	3.26	3.07	99.3
186/reference	1080	1.07	65.1	19.4	205.25	9.83	8.80	2.20	99.1
186/eSAS	920	1.06	66.4		191.52	9.60	8.02	2.42	99.4

Table 1. Key performance metrics of exemplary reference and eSAS single-emitters with resonator length L = 4 mm and varying stripe width W under CW operation at 25°C.

analysis of $I_{\rm th}$ and slope is provided at the end of this section, taking more than 30 measured devices into consideration. The WIAS-TeSCA simulation predicts significantly higher R_s in eSAS devices, i.e. higher slope of the U-I curve (see figure 5(c)), due to current confinement to a smaller area, but this is not validated by the measurement results. As explained in section 2.4, this simulation considers a narrow stripe width device ($W = 20 \ \mu m$) with a single lateral guided mode. It is therefore a sensitive test which exaggerates performance differences, meaning that such a large R_s increase is not expected in practice. Indeed, no significant differences have been observed between the measured U-I characteristics of eSAS and reference devices, an example being the top-left graph of figure 8, indicating that the influence of current confinement on R_s is not strong in broad-area eSAS devices ($W \ge 50$ μ m). Overall, eSAS devices show slightly increased η_{peak} (up to $1.03 \times$) in comparison to their reference counterparts. For example, the η_{peak} of the eSAS device with $W = 90 \ \mu \text{m}$ is 66.5%, compared to 64.8% for the reference device with the same W.

Both reference and eSAS devices with varying W have demonstrated very high DOP (>99%). This is consistent with findings reported in [3, 5], namely that maintaining a high degree of surface flatness, which is valid for both eSAS and reference devices, results in high polarization purity. In terms of beam quality, near-field measurements have demonstrated a significant reduction in w95% in eSAS devices with varying W at varying values of P_{opt} in comparison to their reference counterparts. On the other hand, far-field measurements have produced mixed results, with no clear trend in terms of $\theta_{\ell,95\%}$. Overall, eSAS devices have shown a significant improvement in beam quality compared to reference devices, represented by a consistently lower BPP_{lat}. This results in enhanced lateral brightness ($B_{lat} = P_{op}/BPP_{lat}$) in eSAS devices by up to 21.8, 25.3, and 10% compared to reference devices at W = 50, 90,and 186 μ m respectively. The 90 μ m eSAS SE with the highest measured B_{lat} of 3.07 W/(mm·mrad) at $P_{\text{op}} = 10$ W shows a significant improvement over its reference, and is broadly comparable to the brightest devices with similar dimensions reported to date. For example, 3.5 W/(mm·mrad) at 7 W has been reported from a 90 μ m deep-implanted SE (L = 4 mm), but with a significantly lower η_{peak} of 55% [8]. Minibars with a 5×100 μ m geometry (L = 4–5 mm) have demonstrated ~3.0-3.5 W/(mm·mrad) at 50-70 W. These minibars can be tailored to reach higher values up to 4.8 W/(mm·mrad), but with decreased reliability and robustness due to the increased current and power densities [26].

Using the approach described in [27], a numerical estimate of the reduction of current loss by implementing the eSAS can be obtained. To this end, over 30 SE chips of varying W are mounted and tested. As shown in figure 9(a), the I_{th} values of the mounted SEs are plotted as a function of W, and linear fits of the data points are taken and extended to intercept with the y-axis, giving non-zero $I_{\rm th}$ values at $W = 0 \ \mu m$. These values, which shall be referred to as $I_{th,0}$, represent an empirical estimate of current loss at device edges due to current spreading. It is observed that $I_{\text{th},0}$ is reduced from 269 mA in the reference structure to 109 mA in the eSAS. We thus estimate that the eSAS results in a 59.5% reduction of current loss at device edges at $I_{\rm th}$, which is comparable to the reduction estimated by simulation (65.5%, see section 2.4). With multiple chips measured at each W, average values are calculated for the $I_{\rm th}$ reduction in eSAS devices compared to their reference counterparts, resulting in reductions of 36.8, 34.3, 18.7, and 11.8% at W = 20, 50, 90, and 186 μ m respectively (c.f. 12–16% in BM [12] and 4–12% in LBI BALs [14] with $W = 100 \ \mu m$). It is clear that the influence of the eSAS on I_{th} is stronger in chips with narrower W, where current loss at stripe edges is more significant compared to the current under the stripe. The results also show a larger net benefit of the eSAS compared to the BM and LBI structures in terms of $I_{\rm th}$, but we note that this comparison may also be influenced by the vertical structure, which was not identical in every case.

The slope values of these mounted SE chips are shown in figure 9(b). The differences in slope for devices with $W \ge 50$ μ m are small and lie roughly within the $\pm 1.5\%$ standard error margin (precision limit) reported in [1], which is indicated on the figure. At $W = 20 \mu$ m, the slope is reduced by ~3.5%, which contradicts the slope enhancement predicted by WIAS-TeSCA (see figure 5(c)). The likely cause of this contradiction is the weak lateral waveguiding in these narrow devices, which leads to a poor match between the optical field and the carrier profile, and thus results in increased losses. The weak guiding also causes unstable operation and mode hops, appearing as kinks in the power-current (P-I) characteristics, that are not accounted for in the simulation, where a single strongly-index-guided mode is taken into consideration. Taking all the tested SE chips into consideration, it is clear that



Figure 9. (a) Threshold current I_{th} and (b) slope as functions of stripe width W for over 30 reference and eSAS mounted single-emitter chips under CW operation at 25°C.

the expected slope enhancement could not be experimentally demonstrated in this first realization. Other lateral structuring techniques have demonstrated slope increases in comparison to their references, namely 8-11% in BM [12] and 11-15% in LBI BALs [14] with $W = 100 \ \mu m$. However, upon comparing the absolute values, it appears that the slope values in this work (of both eSAS and reference devices) are comparable to the highest values obtained by BM and LBI devices, rather than their references which have lower slope. Since a reference with one-step epitaxial growth of the ETAS variant used in this realization is not available, it is not possible to discount a possible slope penalty due to etching and regrowth (c.f. 5% reported in [12]). Overall, the first realization of eSAS diode lasers has demonstrated clear performance benefits in terms of I_{th} and BPP_{lat} , but has not shown a clear benefit or penalty in terms of slope, so this remains a topic for further investigation.

4. Summary and conclusions

In this work, high-brightness BALs ($\lambda \approx 940$ nm) with the enhanced self-aligned lateral structure (eSAS) have been demonstrated. In this structure, a current block is introduced in the device edges, to limit the detrimental effects of current spreading and LCA on laser performance. Our design procedure has been described, showing how simulation results and process constraints have been used to set design parameters such as position, materials, thickness and doping concentration of the current block. In comparison to established SAS designs, the current block in our eSAS design contains an additional n-InGaP layer under the n-GaAs layer, enabling precise definition of the etching depth, and is integrated within an ETAS epitaxial design with a thin p-side, allowing the current block to be located close to the active zone without added process complexity. The performance benefits of eSAS devices over standard reference BALs were then estimated using different modeling and simulation tools. To verify the correct implementation of the eSAS in its first realization, we have used blocking quality tests of simple current-blocking structures, in addition to SEM images of processed eSAS BALs. Standard devices with no current blocks have been processed alongside eSAS devices on the same wafers, to be used as references for the eSAS devices to be compared to. Strong reductions in I_{th} and $w_{95\%}$ have been demonstrated in eSAS devices with varying W in comparison to their reference counterparts, thus proving the functionality and effectiveness of the eSAS. Very high DOP values (>99%) have been measured in both eSAS and reference devices, and there have been no clear increasing or decreasing trends in terms of slope and $\theta_{\ell,95\%}$, meaning that the expected improvement in these metrics has not been achieved. Overall, a significant enhancement of B_{lat} by up to 25% along with a slight improvement in η_{peak} by up to $1.03 \times$ have already been demonstrated in this first realization. The eSAS is therefore capable of achieving higher performance than other lateral structuring techniques in GaAs-based BALs, because it allows a significant beam quality enhancement without an efficiency penalty.

Acknowledgment

The authors would like to thank G Erbert, M Weyers, P Ressel, T Kaul, A Zeghuzi and H Lawrenz for their support of this work, and TRUMPF Laser GmbH for funding it.

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